University of Tasmania

High-Performance Microcontroller-Based Transvector-Controlled Pulsewidth Modulator - Induction Motor Drive

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To: Mr. Quang Ha.

I thank you very much for your technical advice to realize and develop ideas of the project.
It is time to say good bye. Many thanks again and best wishes to you and your family.

Dang Trung Nam Tien.

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Abstract :

A fully digitalised transvector control PWM-IM drive system based on the M68HC11 microcontroller is described. The controller receives a digital speed command from a host computer via RS-232 interface. The feedback control system employs a transvector control technique to achieve a high dynamic performance in the estimated frequency range from 5 to 100 Hz. The PWM modulator utilises a computational intensive, uniformly sampled sine wave technique at low frequency region while a look-up table, pattern retrieval method base on the harmonic elimination optimal technique is utilised at high frequency region. The system hardware is mostly based on the programmable counters while system software is completely written in C++.

Acknowledgments.

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Tặng anh Quang để nhớ những ngày ở Hobart.
Cám ơn anh về tất cả những gì anh đã giúp em.
Mong cho anh đạt được tất cả những gì anh muốn trên đường sự nghiệp và thật hạnh phúc Trong cuộc sống.

Em

Dặng Trung Nam Tiến

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Chapter 1 : The IM Drive System - Status and Recent Trends.

The technology of solid-state speed control of induction motor (IM) made great strides during the last decades. Traditionally, IM were considered suitable for constant speed application though complex, inefficient and expensive methods of speed control were known before the advent of the solid-state era. For a long time, dc motor were the workhorses in industry for adjustable speed applications.
The induction motor, especially the cage type, seem to possess many distinct virtues in comparison with dc machine. These relate to lower cost and weight, lower inertia, high efficiency, improved ruggedness and reliability to operate in a dirty and explosive environment due to the absence of commutators and brushes. Some of these virtues are of paramount importance, which makes the IM drive mandatory in several areas of application.
In spite of many virtues of IM, the cost of converters and complexity of control requirements are the main factors which are impeding the widespread application of IM drives in competition with dc drives. Therefore, the project intentionally starts with some discussion of the status and recent trends of IM drive system.

1-1, Power inverter :

1-1-1, Power semiconductor device :

The power semiconductor device is the heart of the power inverter. The first invention of the power semiconductor device were the thyristor in the last 1950's. Gradually, other types, such as triac, gate turn - off thyristor (GTO's), bipolar power transistor (BJT's), power MOS field-effect transistor (MOSFET's), insulated gate bipolar transistor (IGBT's), static induction transistor (SIT's) and MOS-controlled thyristor (MCT's) were introduce. In parallel with the new device evolution, the power rating and switching performance of the existing devices began improving dramatically.
+ Thyristor have traditionally been the workhorse in power inverter. Starting originally with the C35 type (800V, 35A) introduced by GE, the modern light-triggered high-power thyristor (6kV, 35kA) have been involving for more than three decades during the thyristor era. The thyristor application is common ranging from several watts to multimegawatt converter.
+ Triac or bidirectional thyristor were invented by GE almost immediately after thyristor commercialisation and found tremendous popularity for medium power inverter. Except for zero voltage ac line switching, the role of the triac will diminish in the future.
+ The GTO, which is another invention of GE that appeared at almost the same time as the triac, was a glimmer of hope, but soon, its research and application were abandoned, considering that device practically has no future. However, from the late 1970's and early 1980's, a number of Japanese corporations introduced high-power GTO's in the market and substantiated that voltage-fed inverters built with self-controlled GTO's have considerable efficiency, size, and reliability advantages over those with force-commutated thyristor. However, the GTO has large switching loss and shows a second breakdown problem at turn-off that demands a large turn-off snubber. The loss consideration also restricts switching frequency typically below one kHz.
+ Bipolar and field-effect transistor principles were known from the beginning of the solid-state era, but the modern power BJT's and MOSFET's penetrated the market from the mid 1970's. Darlington power transistor modules with built-in feedback

diodes (as high as 1200V, 800A0 gradually pushed the voltage-fed transistor inverter rating up to several hundred kilowatts. Higher switching frequency (several kilohertz) and, consequently, the reduced snubber size were definite advantages over the GTO converter. Power MOSFET's also found a large market acceptance, but because it is majority carrier high-frequency high-conduction drop (especially for high-voltage rating) device, it is dominant in high-frequency low-power applications.
+ The introduction of the IGBT in the early 1980's has brought a visible change in the trend of the power inverter, The IGBT is a hybrid device that combines the advantages of the MOSFET and the BJT. The device is slightly more expensive than BJT's, but the advantages of the higher switching frequency , MOS gate drive, the absence of the second brokendown problem, snubberless operation, reduced the Miller feedback effect, and the availability of the monothilic gate drive with 'smart' capability provides the overall system advantage to the IGBT power inverters.
+ A device that is showing tremendous future promise is the MOS-controlled thyristor (MCT). The MCT is basically a MOS-gated thyristor that can be turned on or off by a small pulse on the MOS gate. The device was announced by GE in November 1988 then was commercially introduced in 1992. Considering that it is new device and there is future evolutionary improvement potential, MCT's are expected to have a significant impact in medium to high power inverter.

1-1-2, Inverter topology.

Converters are generally classified into two types : square wave and pulse width modulated inverter. The square wave inverter was introduced from the beginning of 1970's. It has high efficiency and its simplicity of control has made this class of converter popular in application. However, the disadvantages are that square wave control generates 5th, 7th, 11th ... harmonics that create a rotating magnetic field moving much faster than that of the fundamental frequency and therefore the rotor appears to be stationary to the harmonics. This can be eliminated by using multi-phasing technique, ie more than 6 stepped wave is generated by mixing the phase shifted inverter voltage through a multi-winding transformer or machine. Such a complex and expensive system can be justified only for high power.
The square wave inverters are normally used in low to medium power where the speed ratio is usually limited to 10:1. Recently, this type of drive has largely been superseded by the PWM drive which will be described next.
More recently, the PWM inverters that can compensate harmonics have received wide attention. The key principle of PWM technique is that it keeps dc link voltage uncontrolled by a diode rectifier in the front end and controls electronically the fundamental frequency by using PWM technique. Although harmonic loss is improved significantly in PWM technique, the PWM inverter efficiency is lessened because of many commutation per half cycle and the line current distortion factor is poor with capacitor filter in the dc link. Therefore, the commutation frequency should be increased as permitted by the devices to obtain a good balance between increase of inverter loss and decrees of machine loss. Recently, soft switching have been proposed practically for eliminating the switching loss and considerable amount of research and development are in progress in this area.

1-2, Control of induction motor.

1-2-1, Control technique:

A simple, economic, but low-performance control method of induction motor that is extremely popular in industry is the open-loop V/Hz control technique. A small drift in speed and air-gap flux due to a fluctuation in load torque and supply voltage as well as sluggish transient response, are of no consequence in the majority of application. Scalar speed and position feedback system with inner flux, torque, and current control loops have been used with increased control complexity where improved performance is necessary.

The concept of transvector control, or field oriented control, which was introduced by Siemens Company in the beginning of the 1980's brought on a renaissance in modern high performance control of induction motor driver. This is known as transvector technique because the control implementation is based on vector transformation from rotating to stationary reference frame and vice versa. With transvector control technique, the dynamics of induction motor drives is similar to that of dc motor drives, ie, the transient response is optimal and conventional stability limit does not arise. Therefore, the induction motor-transvector control system has found wide acceptance in industry such as paper mills, textile mills, steel rolling mills, machine tool, servo and robotics.

1-2-2, Modelling and control design.

The control and feedback signal processing of IM drives are extremely complex. This problem arises because the IM dynamics (d-q model) is described by a high-order non-linear multi-variable state-space equations and the converter-IM drives is essentially a discrete system. At a particular point, the system can be linearised on the basis of the small signal perturbation. Then, the conventional linear feedback analytical method, such as the Nyquist and Bode plot techniques, can be applied. However, the linearization method requires considering to all operation points of speed range because when the operation point changes, the poles, zeros and gain of the linearized system will also change, mandating a new set of control parameters for the system. Traditionally, a fixed control structure with a fixed set of control parameters is defined so that the worst-case system performance is acceptable. With the user-friendly simulation program (such as SIMNON, ACSL, MATLAB, etc.) available today, the IM drive system can be studied with computer simulation avoiding the laborious analytical techniques

In the conventional IM control system, the set of control parameters is fixed. This reduces the performance of system because of the changing of motor parameters in operation. In a very high performance IM system, the modern adaptive and optimal techniques are applied. Adaptive control, such as self-tuning regulator, model reference adaptive control (MRAC), and sliding mode control give robust drive performance. The MRAC theory is well developed but is hardly useful for drive control application. However, the principle has recently become popular for estimation of feedback signals, such as torque, flux and speed. Of all the adaptive control methods, the sliding-mode control is somewhat easy to implement, but 'chattering' has been a serious problem. Recent works in this control area relates to adaptive variation of control parameters, hybrid state feedback control, optimisation of trajectory for fast response, and inclusion of low-pass filters in the forward path (to eliminate chatter). Although the literature is abundant in various adaptive and optimal control of IM drives, there is hardly any practical application of this type of IM drive. It is expected that with further research, these drives will find the market place.

On the other hand, many attempts are being made to enhance the drive performance by intelligent, self-learning, self- organising control using expert system. fuzzy logic, and neural network techniques. The discussion on IM control technique will remain incomplete without some discussion of these techniques.

Expert system (ES) is a branch of artificial intelligence that deals with planting human expertise in certain domain in computer program with the object of replacing the human expert. Symbolic processing languages, such as PROLOG and LISP, find favour in expert programs, but for high-speed real-time control, the C or Assembly language can be used. Expert system is potentially a very important tool in IM drive application. Fault diagnostics both on-line and off-line can be based on ES. Automatic design of the converter and total control system is possible using the database of components. Automated simulation study, generation of the static and dynamic model from test data, and system performance test can be performed with the help of ES. Real time performance optimisation control, control reconfiguration, and fault-tolerant control on the basis of on-line diagnostics are also possible with expert system.

Another important tool for IM control system is fuzzy set theory. The theory was introduced by Zadeh in 1965, but only recently, its application has been receiving a lot of attention in Japan. A fuzzy control or estimation algorithm in IM control system embeds the intuition and experience of operator, designer and researcher. It is good in a system where the model is an unknown or ill-defined, complex non-linear multi-dimensional system with a parameter variation problem such as IM or where the sensor signals are not precise. The fuzzy control is adaptive in nature with system parameter variation. The estimation of speed, torque, flux and slip gain tuning can use fuzzy logic, overcoming the parameter variation problem. Unfortunately, there is no systematic analysis and design procedure, and therefore, fuzzy logic-based design may very time-consuming.

The artificial neural network (ANN) is another potentially important tool for IM control system. The term neural network is analogous to the nervous system in the human brain, where a large number of nerve cells are interconnected by input dendrites and axons. The input parallel signals from a layer of cells are processed, and if the output exceeds a threshold, it is propagated to another layer of cells in parallel through the axons. The ANN learning is complex, and various methods, such as back propagation, harmony theory, Bolzman machines, and competitive learning, have been applied. Very recently, several attempts have been made to apply it to PWM-IM control system [13].

It appears that, in the future, the elements of expert system, fuzzy logic and neural network will be combined to gain performance optimisation for IM drive system.

1-3, Microcontroller.

The control system for IM so far are normally implemented using dedicated analog and digital hardware. Recently, however, microprocessor and microcomputer control of IM drives is receiving wide attention because they not only provide simplification of hardware and improvement of reliability but permit performance optimisation of the drive system which could not be possible by hardware control.

The first generation of the microcontroller is 8080 that was introduced by Intel Corporation in 1972. Since then, the technology has gone through an intense evolution in the last two and half decades. At the present, a very dominant member of the Intel family is the 16 bit, signal chip 8096 microcontroller, which is designed for real-time applications. It has a built-in A/D converter that can accept unipolar signals.

With a 12-MHz clock frequency, the 8096 can do a 16 bit addition in 1μs and a 16×16 multiply in 6 μs. Therefore, this microcontroller is expected to find wide application in IM control system.

Other competitors in the market are Motorola, Zilog, Texas Instrument, and National Semiconductor. Although National Semiconductor originally introduced 32 bit architecture in 1988, the age of the 32 bit microcontroller truly started with the introduction of Motorola's 68020. At the present, the prominent members of the 32 bit family are Intel's 80486, Zilog's Z8000, etc.

The advantages of microcontroller in IM drive system seem obvious.

The superiority of microcomputer control over the conventional hardware based control can be easily recognised for complex drive system. The simplification of hardware saves control electronic cost and improves the system reliability. The digital control has inherently improved noise immunity which is particularly important here because of large power switching transients in the converter. The soft control can easily be altered or improved in the future without changing the hardware. Another important feature is that the structure and parameters of the control system can be altered in real time making the control adaptive to the plant characteristics. The complex computation and division taking capabilities of microcomputer make possible to apply the model optimal and adaptive control theories to optimise the drive system performance. In addition, powerful diagnostics can be written in software. Microcomputer is moving at such a fast rate that the use of efficient high level language with large hardware integration already is possible, and possibly, VLSI implementation is the next goal.

What role can the microcontroller play in IM drive system? Practically, all the control functions can be implemented by microcontroller. The application areas may include gate-firing control of phase-controlled converter, closed loop control, non-linearity compensation, programmable set-point commands, system monitoring and warning, and data acquisition. Microcontroller has been used for optimal PWM wave generation of an inverter. Powerful microcontroller are permitting transvector control and optimal and adaptive control in IM drive system. The cost of an IM drive system can be reduced by using cheap sensors and by reconstructing precise signals with the micro's intelligent. In many cases, sensor can be completely eliminated, or redundant sensor information can be provided by observer computation. System reliability can be enhanced by micro-assisted fault-tolerant control. As the microcontroller's speed and functional integration improve, it will be used in real time or quasi real time for simulation of the IM control system.

The microcontroller will play an increasingly important role in system test and diagnostic. The data from a system under test can be captured and processed to determine efficiency, power factor, etc. Automated test can be performed on a system, and structure and parameters can be identified.

In summary, this chapter gives a comprehensive technology status overview as well as recent trends of various converter topology, IM control technique and microcontroller in an IM drive system. It emphases that the cost of the power inverter has been substantially reduced because of the advent of power semiconductor devices. High performance of IM drive system can be achieved by using the PWM technique for inverter and transvector control technique for IM. For very high performance, Expert system, fuzzy logic and neural network promise large potential impact.

Chapter 2 : Induction motor and transvector control

2-1, Induction motor :

2-1-1, Introduction.

A three phase IM contains a three phase distributed winding that are housed in slots on the stationary part of the motor, usually called stator. The rotating part of the machine, or rotor, also contains either distributed three phase winding or a cage of interconnected copper bars that serve as rotor winding connector. When the rotor contains a distributed winding, the three phases of these windings are connected to three slip rings the motor shaft and the motor is known as a would-rotor machine or slip ring machine. When a cage of copper bars is used, these bars are electrically connected by end ring inside the rotor, no electrical connection can be made to them and the motor is known as a squired-cage motor or , more simply, a cage motor.
One set of three phase windings is connected to a three phase voltage supply and this set becomes the primary or excitation (field) windings. With a slip ring motor either stator or rotor windings may act as primary windings, although invariably the stator is used. With a cage motor, only the stator windings can be used as primary windings. The other set of motor windings, known as secondary windings, is not connected to the electrical supply, but is closed on itself. There is no electrical connection between the primary and secondary windings but these are linked magnetically as in a transformer. It is because the secondary e.m.f's and currents are produced by electromagnetic induction that the motor is known as an induction motor.
As with any form of electric motor, the force on the rotating conductor, and hence the motor torque, is proportional to the product of the armature current and the mutual flux in the air gap.

2-1, Steady-state characteristics of Induction motor

When the stator windings of IM is supplied by a balanced sinusoidal three phase ac voltage source of electric speed ω_1 :

$$v_{AB} = \sqrt{2}V_{AB}\sin\omega_1 t = V_L\sin\omega_1 t$$

$$v_{BC} = \sqrt{2}V_{BC}\sin(\omega_1 t + \frac{\pi}{3}) = V_L\sin(\omega_1 t + \frac{\pi}{3}) \qquad (2.1)$$

$$v_{AC} = \sqrt{2}V_{AC}\sin(\omega_1 t - \frac{\pi}{3}) = V_L\sin(\omega_1 t - \frac{\pi}{3})$$

The resulting three phase currents establish a rotating m.m.f wave that result in a flux wave of constant amplitude rotating at a constant speed known as the synchronous speed ω_{ms} :

$$\omega_{ms} = \frac{\omega_1}{P} = \frac{2\pi f_1}{P} \qquad (2.2)$$

P : number of pole pairs.

Under the rotating flux, the rotor of the IM will run at speed ω that is less than the synchronous speed ω_{ms} . The speed difference ω_{ms} - ω is called slip speed and the ratio of the slip speed to synchronous speed is called the per-unit speed S :

$$S = \frac{\omega_{ms} - \omega}{\omega_{ms}} \tag{2.3}$$

At steady state, an IM may be characterised by a per-phase equivalent circuit referred to stator as shown in fig 2.1.

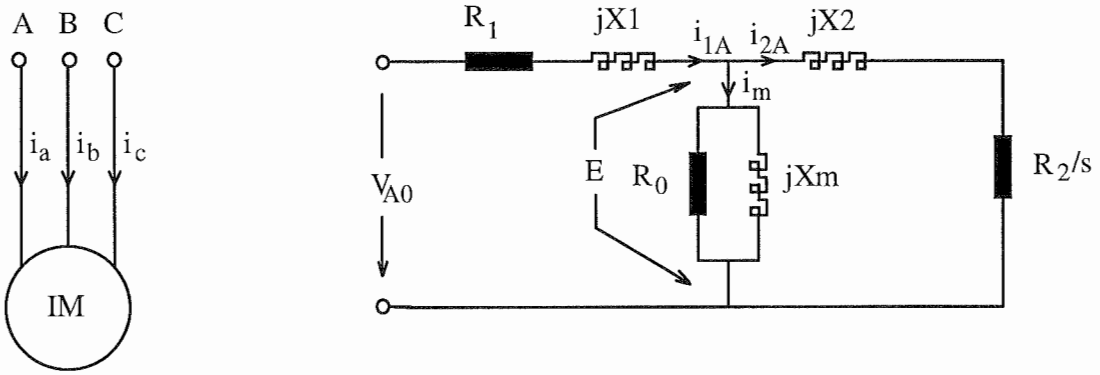


Fig 2.1, Per-phase equivalent circuit of IM (referred to stator)

Suppose that fig 2.1 shown the equivalent circuit of phase A in which v_{A0} is the phase voltage, we have :

$$v_{A0} = \sqrt{\frac{2}{3}} V_L \sin(\omega_1 t + \frac{\pi}{6}) = \sqrt{2} V_{A0} \sin(\omega_1 t + \frac{\pi}{6}) \tag{2.4}$$

and : R1 = per-phase resistance of stator winding, ohm.
jX1 = per-phase leakage reactance of stator winding, ohm.
jXm = per-phase magnetising reactance of the motor, ohm.
R2 = per-phase resistance of rotor winding, referred to stator, ohm.
jX2 = per-phase leakage reactance of stator winding, ohm.

where :

$$R2 = k_r^2 R_{a2} \tag{2.5}$$

$$X_2 = k_r^2 X_{a2} \tag{2.6}$$

$k_r = \frac{n_1}{n_2}$: rotor-stator refer constant. (2.7)

R_{a2} : actual per-phase rotor resistance.

X_{a2} : actual per-phase rotor reactance.

n_1, n_2 : number of effective turn on the stator and rotor.

The equivalent circuit in fig 2.1 can be replaced by its Thevenin' equivalent circuit as shown in fig 2.2.

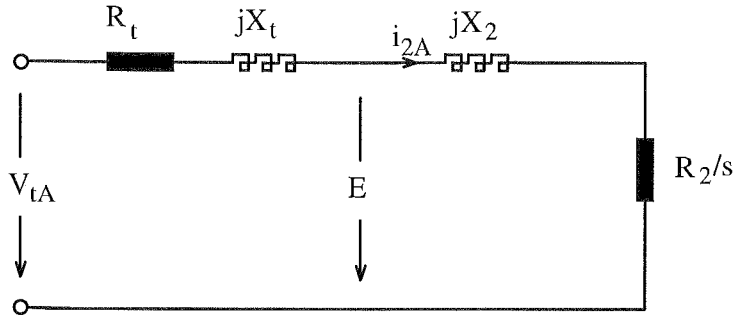


Fig 2.2, Per-phase Thevenin's equivalent circuit of IM

where :

$$v_{tA} = \sqrt{2} V_{tA} \sin(\omega t + \frac{\pi}{6} + \phi_{tA}) \tag{2.8}$$

$$V_{tA} = \frac{V_{AO} X_m}{\sqrt{R_1^2 + (X_1 + X_m)^2}} \tag{2.9}$$

$$\phi_{tA} = \frac{\pi}{2} - \tan^{-}(\frac{X_1 + X_m}{R_1}) \tag{2.10}$$

$$R_t + jX_t = \frac{jX_m(R_1 + jX_1)}{R_1 + j(X_1 + X_m)} \tag{2.11}$$

and R0 is neglected.

From the per-phase Thevenin's equivalent circuit, the following equations can be derived [1, p.207] :

- The speed-torque characteristic equation of IM :

$$T = \frac{3}{\omega_{ms}} \left[\frac{V_{tA}^2 R_2 / s}{(R_t + R_2/s)^2 + (X_t + X_2)^2} \right] \quad \text{(N.m)} \tag{2.12}$$

T = motor output torque.

-Critical motor speed and torque :

$$s_{max} = \pm \frac{R_2}{\sqrt{R_t^2 + (X_t^2 + (X_t + X_2)^2}} \tag{2.13}$$

$$T_{max} = \frac{3}{2\omega_{ms}} \frac{V_{tA}^2}{R_t \pm \sqrt{R_t^2 + (X_t + X_2)^2}} \tag{2.14}$$

- Motor losses :

$$T = \frac{P_m}{\omega} = \frac{P_g}{\omega_{ms}} = \frac{3}{\omega_{ms}} \frac{I_2^2 R_2}{s} \tag{2.15}$$

$$Pm = \text{output power} = 3I_2^2 R_2 (\frac{1-s}{s}) \tag{2.16}$$

$$Pg = \text{air-gap power} = 3I_2^2 \frac{R_2}{s} \tag{2.17}$$

From Eq (2.13), the speed-torque characteristics of an IM can be drawn up when IM is supplied by a rated voltage/frequency source as in fig 2.3, :

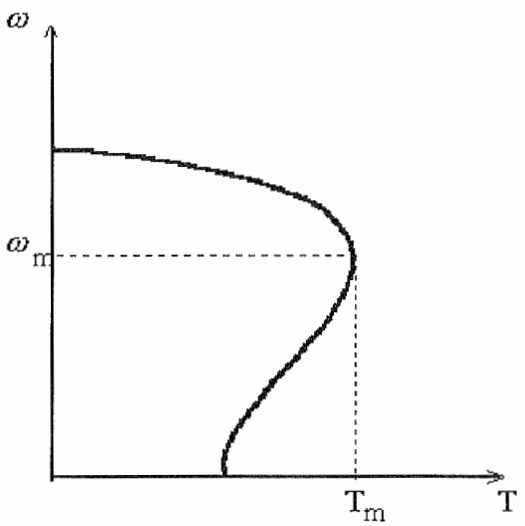


Fig 2.3, Speed-torque characteristic of an IM at steady-state operation.

2-1-3, Variable voltage-frequency controlled IM :

It was shown in eq(2.12) that the synchronous speed ω_{ms} of a three phase IM is proportional to the supply frequency f1. Consequently, the motor speed can be smoothly adjusted from zero up to rated operating speed and higher by increase of the supply frequency f1. However, if the supply frequency f1 is reduced from its rated value while the supply voltage is kept constant, [3, p.236] shows that the motor flux must increase. But operation above the design level would result in excessive core losses and high magnetising current due to an undesirable high level of magnetic saturation. Therefore, in order to maintain operation at the rated flux density when the speed is varied below its rated value, it is necessary to vary the magnitude of supply voltage with variations of its frequency f1.

Controlling IM below rated frequency :

If a is defined as per-unit frequency :

$$a = \frac{f_1}{f_{1\_rated}} \tag{2.18}$$

f1 = frequency of voltage supply.

f_{1_rated} = rated frequency of motor.

it will be less than unit (a<1) when frequency of the voltage supply is smaller than rated frequency of motor ($f_1 < f_{1\_rated}$).
In order to maintain rated motor flux, the e.m.f E must be varied proportionally to frequency f1 [3, p.394] :

$$\frac{E}{f_1} = k = \text{constant} \tag{219}$$

The speed -torque characteristic of IM in this case is derived as following :
The reactance of motor can be expressed in general form :

$$X = \omega_1 L = 2\pi f_1 L = \frac{f_1}{f_{1\_rated}} 2\pi f_{1\_rated} L = aX_{rated}$$

Hence : $E = aE_{rated}$

From the per-phase equivalent circuit of fig 2.1, the rotor current is :

$$I_2 = \frac{E_{rated}}{\sqrt{(\frac{R_2}{as})^2 + X_2^2}} \tag{2.20}$$

where : $as = \frac{a\omega_{ms} - \omega}{a\omega_{ms}}$ (2.21)

The speed-torque characteristic is now obtained from (2.15) and (2.20) :

$$T = \frac{3}{\omega_{ms}} \frac{E_{rated}^2 R_2 / as}{(R_2 / as)^2 + X_2^2} \tag{2.22}$$

Therefore: $s_m = \pm \frac{R_2}{aX_2}$ (2.23)

$$T_m = \pm \frac{3}{2w_{ms}} \frac{E_{rated}^2}{X_2} \tag{2.24}$$

It can be seen that breakdown the torque Tm is constant because both ω_{ms} and X_2 vary proportionally to frequency f1.
The speed-torque characteristic of IM when frequency f1 is changed and the motor flux is kept constant is shown in fig 2.4.

Controlling IM above the rated frequency :

The operation at a frequency higher than the rated frequency takes place at a constant terminal voltage because of the limitation imposed by the voltage supply. Since the terminal voltage is maintained constant, the flux decreases in the inverse ratio of pu frequency a. The motor, therefore, operates in the field weakening mode.

The torque expressions for the operation in this range of frequency f1 are obtained by substituting $a\omega_{ms}$ for ω_{ms} and $a(X_t + X_2)$ for $(X_t + X_2)$ in Eq (2.12) and (2.17) , respectively:

$$T = \frac{3}{\omega_{ms}}\left[\frac{V_{tA}^2 R_2 / as}{(R_t + R_2/s)^2 + a^2(X_t + X_2)^2}\right] \quad \text{(N.m)} \quad (a>1) \qquad (2.25)$$

$$T_{max} = \frac{3}{2a\omega_{ms}} \frac{V_{tA}^2}{R_t \pm \sqrt{R_t^2 + a^2(X_t + X_2)^2}} \qquad (2.26)$$

Since a > 1, the breakdown torque Tm decrease with the increase in frequency and speed.
The speed-torque curves for IM in the field weakening mode are shown in fig 2.4 [2].

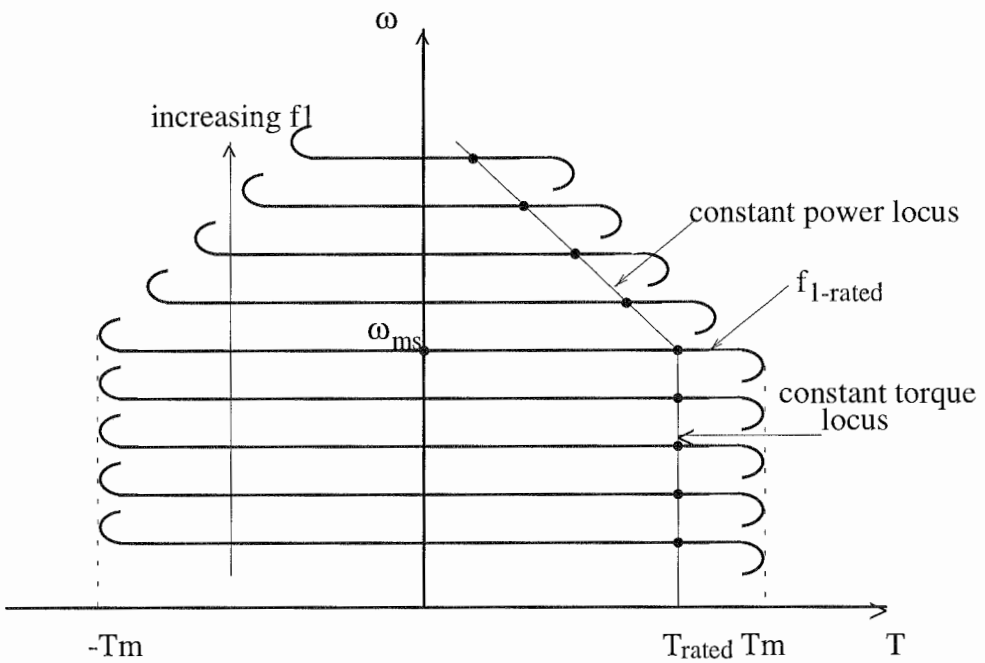


Fig 2.4, Speed-torque characteristic for variable frequency control of IM

Fig 2.4 also depicts the torque and power capabilities for a given stator current and for frequency below and above the rate frequency (dot lines). When the stator current has the maximum permissible value, these will represent the maximum torque and power capabilities of the IM.

2-2, Transvector control

Many different control techniques for controlling an IM has been popular used for a long time [5] : the constant voltage/frequency control, the constant voltage/frequency control with slip regulation, independent torque and air gap flux control (bang bang control, etc. These methods can be classified in to a group called voltage/frequency control that is simple and economical but can be only used for low-performance applications.

In industry application, a high-performance drive system is highly awaited. In this regard, the transvector control technique for the IM is used.

This chapter will analyse the basic control concepts of the transvector technique, then describes its application in PWM-IM drive system.

2-2-1, Transvector control technique.

To analyse transvector control, the operation of IM is considered in the reference frame rotating synchronously with the synchronous electric speed [6] . By such a way, the air gap flux in an IM can be considered as the flux vector $\overline{\Psi}$ rotating with synchronous speed ω_1. Next, the flux vector $\overline{\Psi}$ is considered as an interaction of stator and rotor voltages and currents $\bar{u}_1$, $\bar{i}_1$ and $\bar{i}_2$. By this discussion, the balance voltage equations of IM in the reference frame rotating at constant speed ω_1 are :

$$\bar{v}_1 = R_1\bar{i}_1 + p\overline{\Psi}_1 + j\omega_1\overline{\Psi}_1. \tag{2.27}$$

$$0 = R_2\bar{i}_2 + p\overline{\Psi}_2 + j(\omega_1 - \omega)\overline{\Psi}_2 \tag{2.28}$$

$$\overline{\Psi}_1 = L_1\bar{i}_1 + M\bar{i}_2 \tag{2.29}$$

$$\overline{\Psi}2 = L_2\bar{i}_2 + M\bar{i}_1 \tag{2.30}$$

$$T = PRe(j\overline{\Psi}_2\bar{i}_2^*) \tag{2.31}$$

where : p is derivative operator.
ω is motor speed.
$\overline{\Psi}_1$, $\overline{\Psi}_2$ are stator and rotor flux.
L1, L2 are stator and rotor leakage inductances.
M is the mutual (or magnetising) inductance :

$$M = \frac{3}{2}L_m$$

All the rotor quantities are referred to stator.

If a coordinate system with d and q axis is fixed in the rotating reference frame, a certain vector $\overline{N}$ can be decomposed along the d and q- axis as in fig 2.6. Here, $\overline{N}$ can be $\bar{v}_1, \bar{i}_1, \bar{i}_2, \overline{\Psi}_1$ or $\overline{\Psi}_2$ and θ is angle between rotating reference frame (d and q axis) and reference frame fixed in stator (α and β axis).

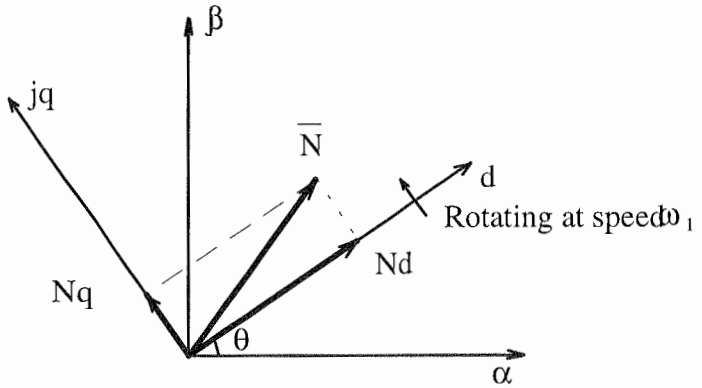


Fig 2.6, Decomposed vector N along d and q axis

Decompose equation system (2.27) through (2.32) along d and q axis, gives :

$$v_{1d} = R_1 i_{1d} + p\Psi_{1d} - \omega_1 \Psi_{1q} \quad (2.32)$$

$$v_{1q} = R_1 i_{1q} + p\Psi_{1q} + \omega_1 \Psi_{1d} \quad (2.33)$$

$$0 = R_2 i_{2d} + p\Psi_{2d} - (\omega_1 - \omega)\Psi_{2q} \quad (2.34)$$

$$0 = R_2 i_{2q} + p\Psi_{2q} + (\omega_1 - \omega)\Psi_{2d} \quad (2.35)$$

and

$$\Psi_{1d} = L_1 i_{1d} + M i_{2d} \quad (2.35)$$

$$\Psi_{1q} = L_1 i_{1q} + M i_{2q} \quad (2.36)$$

$$\Psi_{2d} = L_2 i_{2d} + M i_{1d} \quad (2.37)$$

$$\Psi_{2q} = L_2 i_{2q} + M i_{1q} \quad (2.38)$$

The principle of the transvector control lies on the method to control i_{1d} and i_{1q} *currents so that the d-axis coincides with the rotor flux* $\overline{\Psi}_2$ as shown in fig 2.7.

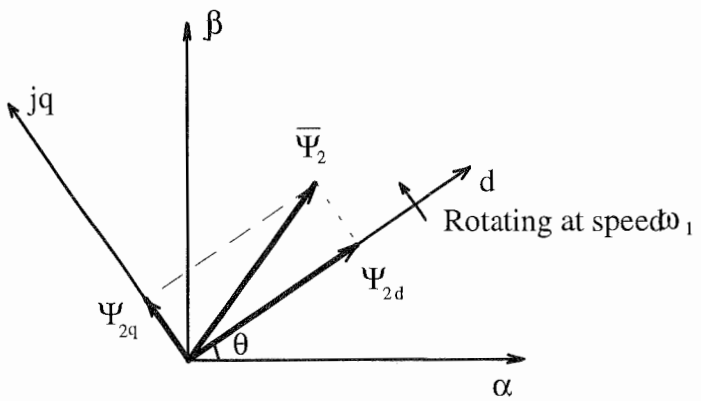


Fig 2.7, Principle of transvector control : $\psi_{2d} \equiv$ d-axis.

As a result :

$$\Psi_{2d} = L_2 i_{2d} + M i_{1d} = \Psi_2 \quad (2.40)$$

$$\Psi_{2q} = L_2 i_{2q} + M i_{1q} = 0 \quad \Rightarrow i_{2q} = -\frac{M}{L_2} i_{1q} \quad (2.41)$$

and : $$\frac{d\Psi_{2q}}{dt} = 0 \qquad (2.42)$$

From (2.41) and (2.37) :

$$0 = R_2 i_{2d} + p\Psi_2 \qquad (2.43)$$

$$\Rightarrow i_{2d} = -\frac{1}{R_2} p\Psi_2 \qquad (2.44)$$

Inserting (2.44) into (2.40), gives :

$$\Psi_2 = -\frac{L_2}{R_2} p\Psi_2 + M i_{1d}$$

or $$\Psi_2 (1 + \frac{L_2}{R_2} p) = M i_{1d} \qquad (2.45)$$

Also, from (2.30) and (2.41) :

$$T = -P\Psi_2 i_{2q} = \frac{PM}{L_2} \Psi_2 i_{1q} \qquad (2.46)$$

Equations (2.45) and (2.46) express the fundamentals of the transvector control technique :

* The rotor flux transients are determined only by the stator current i_{1d} along the same d-axis, and the transients decay with the rotor time constant T2=L2/R2. Hence, in context of transvector control, i_{1d} is called magnetising current.

* The expression for the torque is similar to that of a separately exited dc motor, ie it can be controlled by controlling independently rotor flux Ψ_2 and current i_{1q} . Hence, the stator current component i_{1q} is called the torque current in the present context.

* If the rotor flux Ψ_2 is kept constant, it follows from (2.45) that for $p\Psi_2 = 0$,

$$\Psi_2 = M i_{1d} \qquad (2.47)$$

Equation (2.47) implies that there is no rotor transients and thus the torque current command is instantaneously translated as a torque command. Thus, an ideal response is obtained.

* The transvector can be expanded into the field weakening mode in which the motor speed is higher than rated the motor speed, the voltage at the inverter input is kept constant and the rotor flux is decreased. It can be seen that for transvector control, decreasing the magnetising current i_{1d} , at a constant voltage input, leads to a higher stator frequency ω_1 . For a constant torque current, per-unit speed S must be constant, thus higher speeds are obtained : $\omega = \omega_1 (1 - S)$.

Since the torque is given by (2.46), lowering the magnetising current i_{1d} and keeping the torque current i_{1q} constant will result in reduction in the torque, and hence in

slower speed response. An increasing in the torque to obtain a higher torque is possible by increasing S up to the limit imposed on the total stator current :

$$|i_1| = \sqrt{\frac{2}{3}(i_{1d}^{\ 2} + i_{1q}^{\ 2})}$$

By discussion mentioned above, the control law for rotor flux and magnetising current is drawn up as in fig 2.7

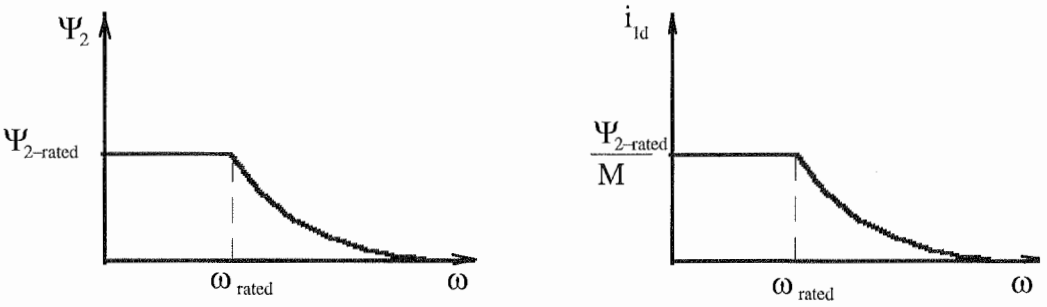


Fig 2.7, Control strategy for current i_{1d}

In the summary, the transvector control technique can be described as following :
a) Controlling currents i_{1d} and i_{1q} so that the d-axis of the synchronous rotating reference frame coincides with the rotor flux Ψ_2. For this, substituting (2.41) into (1.45) to obtain control strategy for i_{1q} and i_{1d} :

$$\omega_1 - \omega = \frac{R_2}{L_2}\frac{i_{1q}}{i_{1d}} \qquad (2.48)$$

b) The IM now can be controlled as dc motor, ie by controlling independently the rotor flux Ψ_2 and the torque current i_{1d} .When IM is controlled below rated frequency $\omega_{1\text{-rated}}$, the rotor flux Ψ_2 is kept constant and equal to its rated value (E / f = const).In contrast, when IM is controlled above the rated frequency $\omega_{1\text{-rated}}$, the rotor flux Ψ_2 must be decreased as in fig 2.7.

2-2-2, Coordinate changer :

a, Coordinate changer from static frame to synchronous rotating frame :

In practice, it is necessary to transfer current vector from real time system to static and synchronous rotating system.
Three real time line current $i_a(t), i_b(t), i_c(t)$ are first interpreted into static reference frame by the following formulas :

$$i_{1\alpha} = \sqrt{\frac{2}{3}}(i_a - \frac{1}{2}i_b - \frac{1}{2}i_c) \qquad (2.49)$$

$$i_{1\beta} = \frac{1}{\sqrt{6}}(i_b - i_c) \qquad (2.50)$$

Next, the current in static reference αβ frame can be changed into synchronous rotating dq frame :

$$i_{1d} = i_{1\alpha}\cos\theta_1 - i_{1\beta}\sin\theta_1 \tag{2.51}$$

$$i_{1q} = i_{1\alpha}\sin\theta_1 + i_{1\beta}\cos\theta_1 \tag{2.52}$$

Equations (2.49) through (2.62) are calculated with help of fig 2.8 [6].

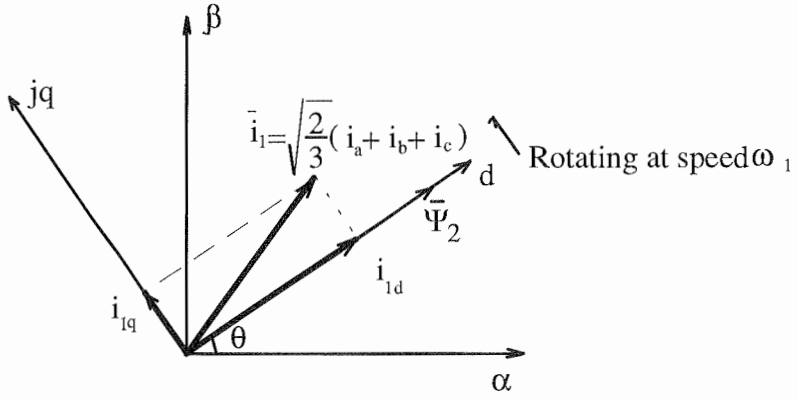


Fig 2.8, Interpretation between αβ frame and dq frame

b, Coordinate changer from synchronous rotating dq frame to static αβ frame.
In many cases, it is necessary to convert a certain parameter from synchronous rotating dq frame to static αβ frame.
Consider the reference voltage expressed in the dq axis in the form of two components V_{1d}^{ref} and V_{1q}^{ref} :

$$v_1^{ref} = V_1^{ref}\sin(\omega_1 t + \theta)$$

$$V_I^{ref} = \sqrt{(V_{1d}^{ref})^2 + (V_{1q}^{ref})^2}$$

and three real time phase voltages are obtained from [6, p.166] :

$$v_{AO}^{ref} = \sqrt{\frac{2}{3}}(V_{1d}^{ref}\cos\theta_1 - V_{1q}^{ref}\sin\theta_1) \tag{2.54}$$

$$v_{BO}^{ref} = \sqrt{\frac{2}{3}}(V_{1d}^{ref}\cos(\theta_1 + 120) - V_{1q}^{ref}\sin(\theta_1 + 120) \tag{2.55}$$

$$v_{CO}^{ref} = \sqrt{\frac{2}{3}}(V_{1d}^{ref}\cos(\theta_1 - 120) - V_{1q}^{ref}\sin(\theta_1 - 120) = -(v_{AO}^{ref} + v_{BO}^{ref}) \tag{2.56}$$

2-2-3, PWM-IM transvector control drive system :

The PWM and transvector control technique can be combined to produce a high quality PWM-IM drive system.

Concerning flux vector detection, the direct sensing method of the air gap flux by the use of Hall probes is most desirable in theory. From the viewpoint of practical application, this method suffers from high cost and unreliability of the measurement. From this regard, the indirect sensing methods of the rotor flux vector has been developed, which can be divided into two groups. In the first group, the rotor flux vector is obtained by integrating the induced voltage detected directly via sensing coils or calculated indirectly from the stator current and voltage. This method suffers from the inaccuracy of the flux estimation in the low speed region arising from the inaccuracy of the integration. In the second group, the rotor flux vector is estimated from stator currents and rotor speed on the basis of the rotor circuit equations of an IM in the synchronously rotating reference frame with rotor flux vector. Since this method does not require any integration, the rotor flux vector can be estimated even in the standstill. The major weakness of this method is the sensitivity of the estimation to change of rotor parameters, such as rotor resistor, arising from a magnetic saturation and a change of temperature.

On the other hand, in order to realise the high response of current control (to ensure the actual stator current must be adjusted instantaneously and precisely according to their reference current. A fast switching PWM inverter with a local feed back loop is usually utilised for the approximate current control and is sufficient for many industrial applications. However, the high gain current controller is generally required to compensate for the induced voltage. Otherwise, the amplitude and phase error between the actual stator current and its reference become no longer negligible, especially in the high speed region, which deteriorates the vector performance. On the contrary, the high gain current loop produces high acoustic noise, unless the switching frequency of the PWM inverter is extremely high (over 20 kHz). To overcome this problem, another type of current control has been developed in which the stator current are transformed into two dc components, that are, a magnetising current component and a torque current component, and then these two dc components are controlled, respective to transvector control law.

This section describes a microprocessor based high performance transvector control system in which the indirect rotor flux estimation method and the dc current component method are employed.

Fig 2.10, and 2.11, show the configuration of the PWM-IM transvector control system. It can be seen that the system is composed of a current and speed detection, a speed controller, two current controllers, a PMW calculation, a PWM generation, and a transistor inverter. Here, the main parts of system are discussed.

* Current detection block receives and decomposed three real time line current $i_a(t), i_b(t), i_c(t)$ into two current components : the torque current i_{1q} and magnetising current i_{1d} (Eq(2.48) to (2.50)). These current components must be controlled independently by the transvector control algorithm.

* Speed control block gets the reference speed ω^{ref} from host computer and actual speed ω from speed detection. Its output is the reference torque current i_{1q}^{ref} .

* Non-linear flux block is used to control magnetising reference current i_{1d}^{ref} . (fig 2.7). If the actual speed ω is below the rated motor speed ω-rated, i_{1d}^{ref} is kept constant in

order to keep rotor flux Ψ_2 constant. When the motor speed ω increases beyond ω-rated, i_{1d}^{ref} must be reduced.

* Rotor flux position block controls position of the rotor flux Ψ_2 to ensure transvector control algorithm : rotor flux must coincide with d-axis of synchronous rotating frame. From (2.48) :

$$\omega_1^{ref} - \omega = \frac{R_2}{L_2}\frac{i_{1q}}{i_{1d}} \qquad (2.57)$$

* Current limiter : in order to protect the transistor PWM inverter from over current, a current limiting function is usually necessary. Here,(in addition to the conventional maximum current limiter in the digital PWM circuit), the current limiting method is also employed, which limits the maximum amplitude of the stator current reference. in fig 2.8, the magnetising current component reference i_d and the torque current component reference i_q are given as the output of the flux and speed controller, respectively. The explicit expression of the stator current reference is not obtained in this system. Usually the limiters with constant limit value are constituted in order to limit the maximum value of i_d and i_q. However, the disadvantage of these constant limit value is, for instance, that the magnetising current is suppressed under the constant value, even when the IM is lightly loaded, that is, the value of the i_q is small. This may deteriorates the performance of the transvector control.

The amplitude of the stator current reference I_1 is expressed as,

$$I_1^r = \sqrt{\frac{2}{3}(i_d^{r\,2} + i_q^{r\,2})}$$

The value which should be watched is not i_d or i_q, but I_1. From this reason, the variable current limiting method is employed here. Fig 2.9, shows block diagram of the variable current limiter.

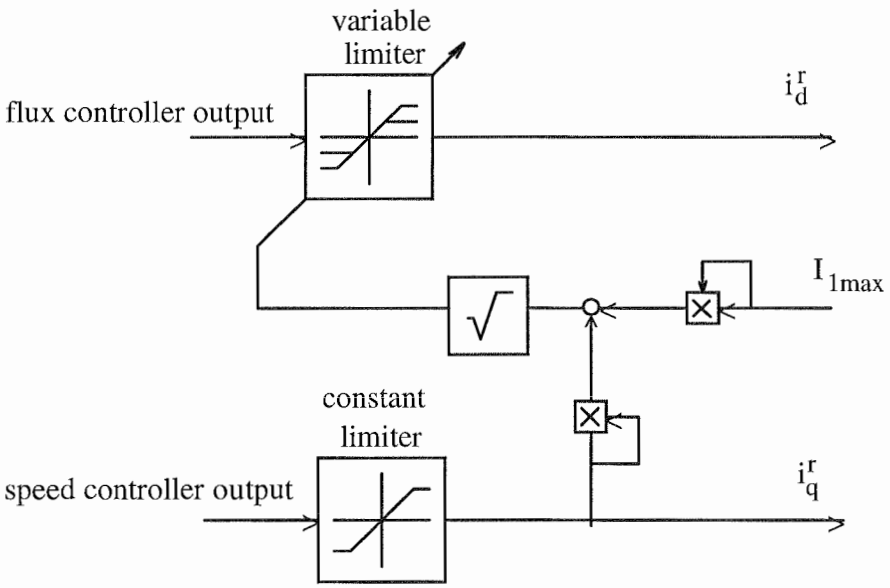


Fig 2.9, Block diagram of variable current limiter.

This limiter enables the system to control i_{1d}^{r} in response to i_{1q}^{r} in order to limit the stator current reference so that it does not exceed the preset maximum value $I_{1\text{-}max}$. It is of course necessary to put the minimum value in the variable limiter of i_{1d}^{r} .

* Two current controller - the magnetising current component controller and torque current component controller- are used to achieve a good performance of system in both steady state and transient operation. Since the quantities to be adjusted by these controllers are dc quantities, conventional PI control technique can be successfully employed.
* Two reference voltage from current controllers are sent to PWM calculation block where time delay and pulse width time PWM signal are determined.
* Depending on the time delay and pulse width time calculated from the PWM calculation block, the PWM generation block produces PWM signals. Then, PWM signals are amplified and sent to the base gates of power transistor of inverter.

In conclusion, this chapter overviews the steady-state characteristics of an IM as well as the basic concepts of the transvector control. It shows that if the stator voltage and current of an IM are converted from stationary reference frame to the synchronously rotating reference frame, the IM will behave like a separately exited dc motor, ie motor flux and torque can be controlled independently. Therefore, the high dynamic performance of the IM drive system can be achieved with the transvector control technique.

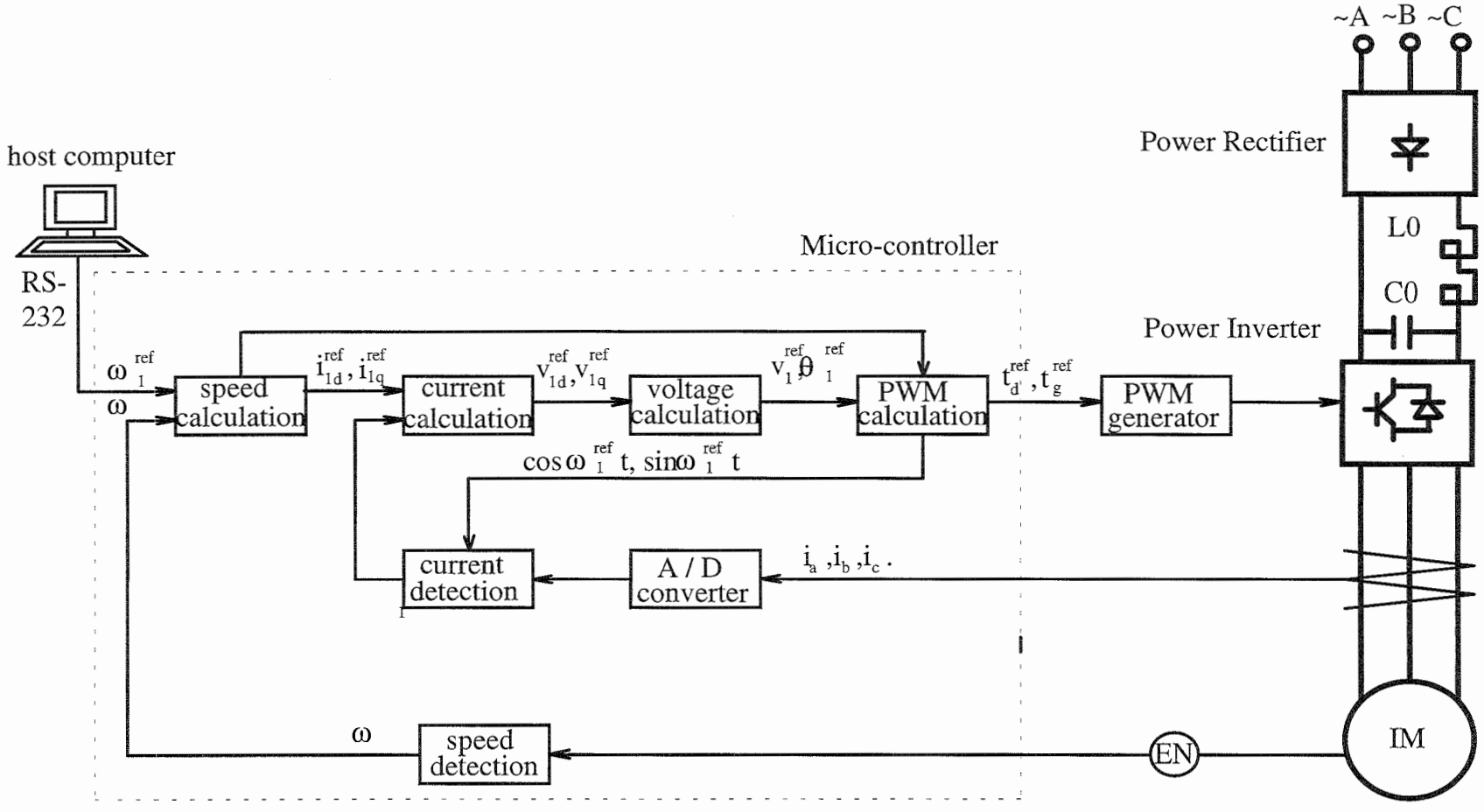


Fig 2.10, PWM-IM system configuration

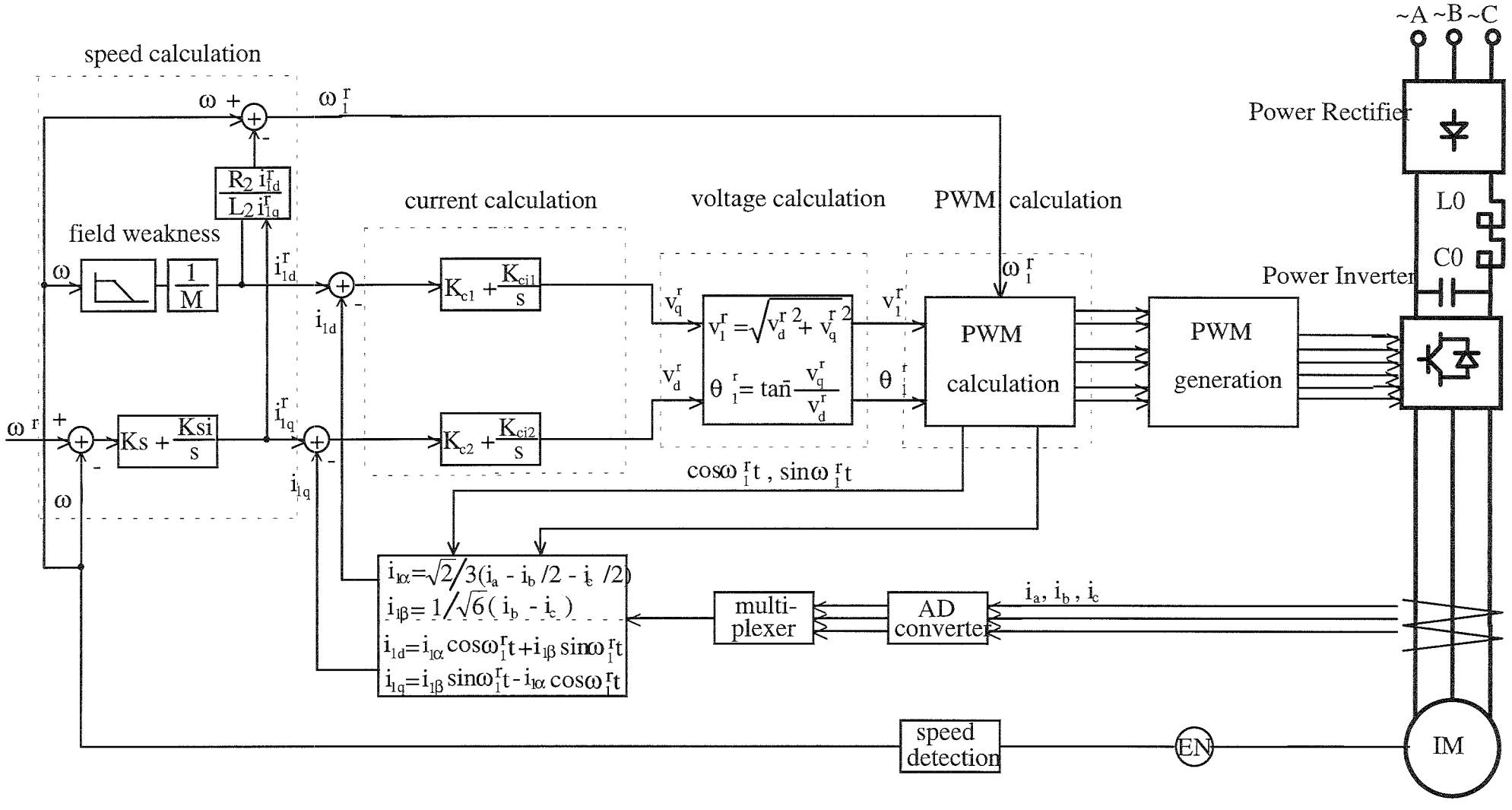


Fig 2.11, Block diagram of the PWM-IM system configuration

Chapter 3 : Dynamics of PWM-IM drive system.

3-1, Introduction :

The dynamics of PWM-IM drive system is extremely complex because of the non-linearity and discrete time nature of the inverter-motor system. For this reason, when a control strategy is developing, it is usually practice to simulate the drive system on the computer and study the performance in detail before proceeding to build a breadboard.

As shown in fig 2.11, the IWM-IM drive system contains three controller : one is to control the reference speed (speed controller) and two the others are used to control the magnetising and torque current (current controllers).The problem is what values of the control parameters the system will satisfy the desired dynamic performance. This chapter considers the steps involving the controller design.

There are two main methods to design a digital controller. In the first method, the control design is done as a continuous control system in the s-plane and then simulated in the form of digital system. The second method determines directly the digital controller in the z-plane.

The project employs the first design procedure using frequency response technique to drive satisfactory control parameters. This procedure totally ignores the fact that a sampler and digital computer could influence on the dynamic response and steady state error of real time digital system. Therefore, the last section of this chapter will discuss these effects on implementation of real time discrete system.

Basically, the response of closed loop system to unit step input has the form as shown in fig 4.1.

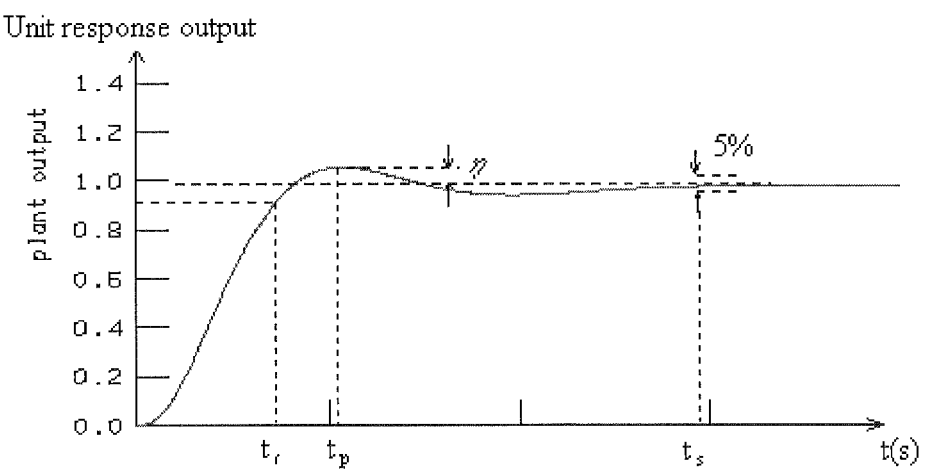


Fig 3.1, Unit response specific

Here :

tr = rise time : time takes the system to reach the vicinity of new set point.

ts = settle time : time takes the system to decay.

tp = peak time : time takes the system to reach the maximum overshoot point.

η = overshoot : is the maximum amount the system overshoots its final value divided by its final value. Overshoot η is often expressed as a percentage.

Normally, these requirements are given by customer. In this project, these specifications are supposed as :

+ tr <= 0.2 s
+ ts <= 0.5 s
+ η <=10% .

3-2, Mathematic model of the PWM-IM drive system.

The first step in control design is to model the overall system. Depending in the actual system, a system can be modelled in the form of mathematical equation, state variable, block diagram , state space or their combination. In this project, the mathematical equation and block diagram method are combined to model the PWM_IM vector control system.

3-2-1, Mathematic model of induction motor IM :

The dynamic properties of an IM as a control plant can be described by a set of non-linear differential linking stator and rotor currents and voltages with the mechanical quantities (torque, speed and angular position).

As discussed in chapter 2, an IM can be described by voltage equations in the synchronous rotating reference dq frame (Eq (2.31) through (2.34)).

Substituting Ψ_{1d}, Ψ_{1q} from (2.35) and (2.36) into (2.31) and (2.32), the voltage equations of an IM in the dq frame can be written in the form of state-space vector [ref 10]:

$$\begin{vmatrix} V_{1d} \\ V_{1q} \\ 0 \\ 0 \end{vmatrix} = \begin{vmatrix} R_1 + pL_\sigma & -\omega_1 L_\sigma & p\dfrac{M}{L_2} & -\dfrac{M}{L_2} \\ \omega_1 L_\sigma & R_1 + pL_\sigma & \omega_1 \dfrac{M}{L_2} & \dfrac{M}{L_2} \\ -\dfrac{MR_2}{L_2} & 0 & \dfrac{R_2}{L_2} + p & -(\omega_1 - \omega) \\ 0 & -\dfrac{M}{L_2} & -(\omega_1 - \omega) & \dfrac{R_2}{L_2} \end{vmatrix} \begin{vmatrix} i_{1d} \\ i_{1q} \\ \Psi_{2d} \\ \Psi_{2q} \end{vmatrix} \qquad (3.1)$$

In addition, from (2.30) :

$$T = -P(\Psi_{2d} i_{2q} - \Psi_{2q} i_{2d}) \qquad (3.2)$$

where : P = number of pole pairs.

$$L_\sigma = \frac{L_1 L_2 - M^2}{L_2} \qquad (3.3)$$

M = mutual inductance.

If IM is controlled by transvector technique, the equations (2.39) through (2.47) must be satisfied and the rotor flux vector will coincide with d axis of dq frame. Therefore :

$$\Psi_{2d} = \Psi_2$$
$$\Psi_{2q} = 0$$

If this condition is held, the system (3.1) reduces to :

$$\begin{vmatrix} V_{1d} \\ V_{1q} \\ 0 \\ 0 \end{vmatrix} = \begin{vmatrix} R_1 + pL_\sigma & -\omega_1 L_\sigma & p\dfrac{M}{L_2} \\ \omega_1 L_\sigma & R_1 + pL_\sigma & \omega_1 \dfrac{M}{L_2} \\ -\dfrac{MR_2}{L_2} & 0 & \dfrac{R_2}{L_2} + p \end{vmatrix} \begin{vmatrix} i_{1d} \\ i_{1q} \\ \Psi_2 \end{vmatrix} \qquad (3.4)$$

and the generated torque is given as :

$$T = -P\Psi_2 i_{2q} = \frac{PM}{L_2}\Psi_2 i_{1q}) \qquad (3.5)$$

From eq (3.4) and (3.5), the block diagram of IM controlled by transvector technique can be drawn up as fig 3.2 . [10].

3-1-2, Model of the closed loop system :

The block diagram of the feed back control system has been discussed in chapter 2 (fig 2.11). If converter is considered as a proportional block with gain K :

$$K = \frac{V_d}{2\sqrt{2}V_T} \qquad f_1 \le f_{1\text{-rated}}$$

and : $$K = \frac{\sqrt{2}V_d}{\pi} \qquad f_1 > f_{1\text{-rated}}$$

The model of closed loop PWM-IM drive system with transvector control can be shown as in fig 3.3 and fig 3.4. Parameters of proposed motor is shown in appendix A.

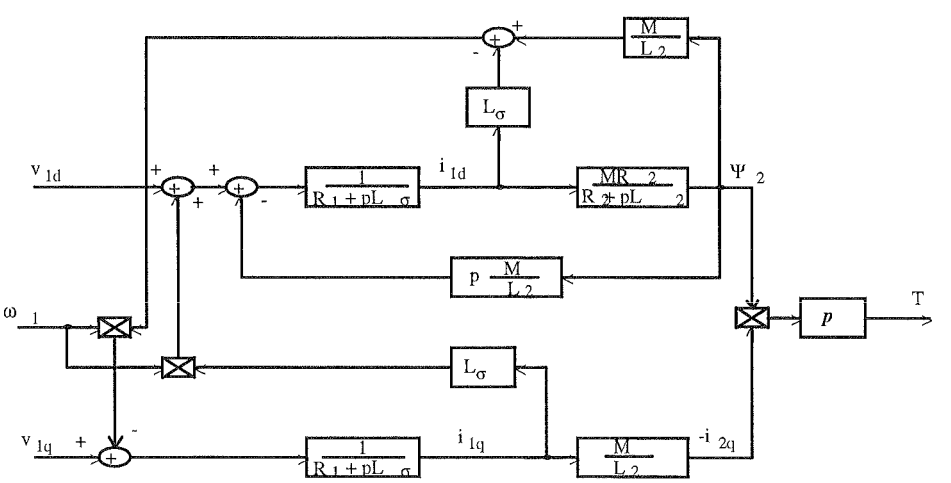


Fig 3.2, model of transvector controlled IM .

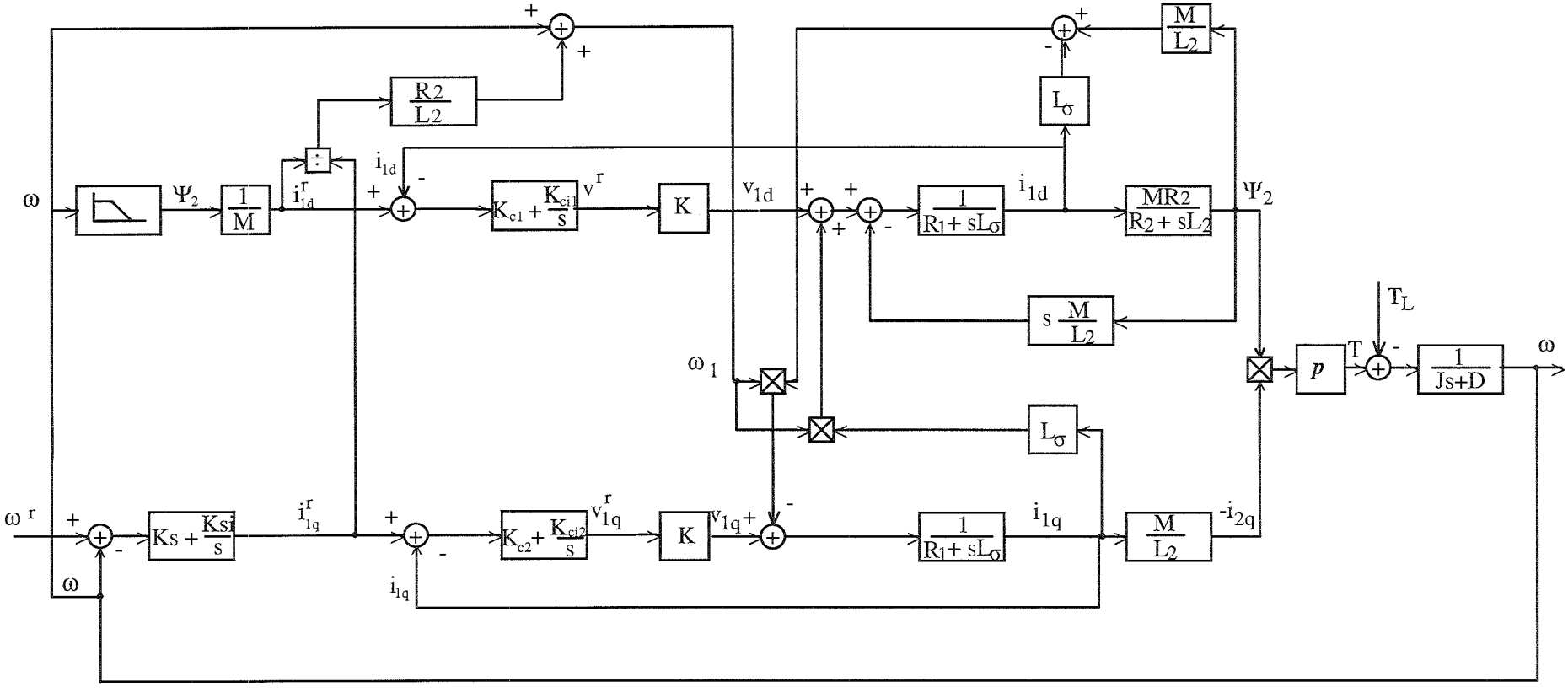


Fig 3.3, Model of closed loop PWM-IM system

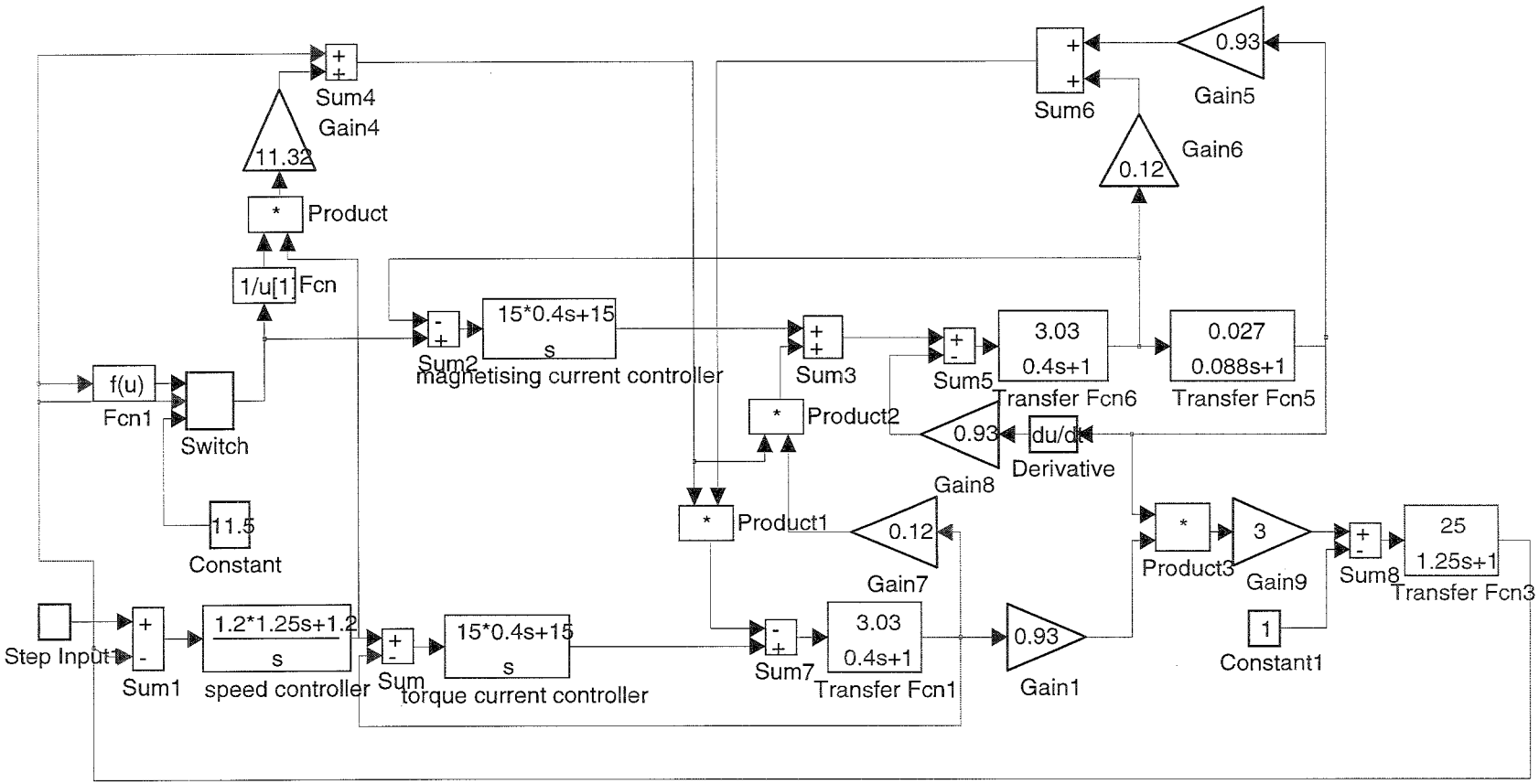


Fig 3.4, System simulation on MATLAB

3-3, Control design :

It can be seen that the transvector controlled PWM-IM system is described by a high-order non-linear multi-variable state-space equation. Therefore, its control and feedback processing is very complicated. To simplify problem, the conventional design method suggest that the system can be linearized on the basis of the small signal perturbation at a particular operating point and then the conventional feedback analytical methods such as the Nyquist and Bode plot technique can be applied. However, if the operating point changes, the poles, zeros and gain of the linearized system will also change, mandating a new set of control parameters for the system. Therefore, the conventional method requires to check and tune control parameters, theoretically, at all operating point of the speed range, then a fixed control structure with a fixed set of control parameters is determined so that the worse-case system performance is acceptable.

With the availability of user-friendly simulation software packagess such as SIMNON, ACSL, MATLAB, etc, a new method is suggested to avoid such laborious design technique.

It is clear that there is a strong coupling between stator current component and stator voltage component via motion voltage. In order to decouple the motional voltage in the reference voltage, in the proposed method, the motion induced coupling voltages are considered as disturbances to reference voltage. By such a way, two current loops become independent and can be synthesised as linear loops with conventional linear feedback analytical methods.

The synthesis of the speed loop is more complicated due to non-linearity of the system and needs helps of computer. It first is designed by hand, ignores the effects of the rotor flux and then the system is simulated by simulink tool of MATLAB software package to check and tune the parameters of the controllers at all the most important points of the speed region until specified requirements of the system are met.

3-3-1, Overview of control design :

There are many methods that can be used to design a controller such as root locus, frequency response, pole-zero placement, state-space, etc. In this project, the frequency response method is chosen to design the current controllers. The principle of the frequency response method is outlined as follows :

In terms of the frequency response, the transfer function of a system can be expressed by a magnitude $| H(\omega) |$ and a phase $| \varphi(\omega) |$ curve respect to frequency ω. These curves are introduced by Bode (1960). By using Bode plot, the stability and dynamic response of system can be entirely analysed through some important factors related to Bode plot diagram. They are :

+ Gain margin GM : is defined as the difference between 1 and $| H(\omega) |$ curve at which the gain of the system is less than the neutral stability value (phase curve crosses 180°.)

+ Phase margin PM : is the difference between $| \varphi(\omega) |$ curve and -180° when magnitude curve crosses 1.

The stability and dynamic response of the system now can be stated as :

* The system is stable when | GM |>=1 or PM >=0.
* Damping of the system decreases when PM increases.

In order to apply the Bode plot diagram technique to design a controller, a dummy function must be introduced depending on the required specifications. If second order could satisfy requirements, the dummy function will has the form :

$$H_d(s) = \frac{K_0}{s(T_0 s + 1)} \tag{3.6}$$

The formulas related to parameters of the second order dummy function and system specifications are [14] :

$$T_0 = \frac{1}{2\xi\omega_n} \tag{3.7}$$

$$K_0 = T_0\omega_n^2 \tag{3.8}$$

where :

ξ = damping ratio : $$\xi = \frac{\ln\eta}{\sqrt{\pi^2 + \ln^2\eta}} \tag{3.9}$$

ω_n = undamped natural frequency : $$\omega_n = \frac{\pi}{t_p\sqrt{1-\xi^2}} \tag{3.10}$$

After the dummy function is determined, the parameter of the controller is somehow calculated so that its Bode plot of the closed loop system is closed to the Bode plot of the dummy function in the range (+15 dB, - 15 dB)

3-3-2, Torque current loop :

In the case of the current loop, the overshoot is permitted up to 25% while the fast response is necessary. Suppose that η = 20% and tp = 0.1s are required, the dummy function of torque current loop is derived from (3.6) through (3.10) (appendix B):

$$H_d(s) = \frac{30}{s(0.0167s + 1)} \tag{3.11}$$

The transfer function of the open loop torque current (without PI controller) is obtained from the torque current block diagram shown in fig 3.3 :

$$H_d(s) = \frac{3.31}{0.4s + 1} \tag{3.12}$$

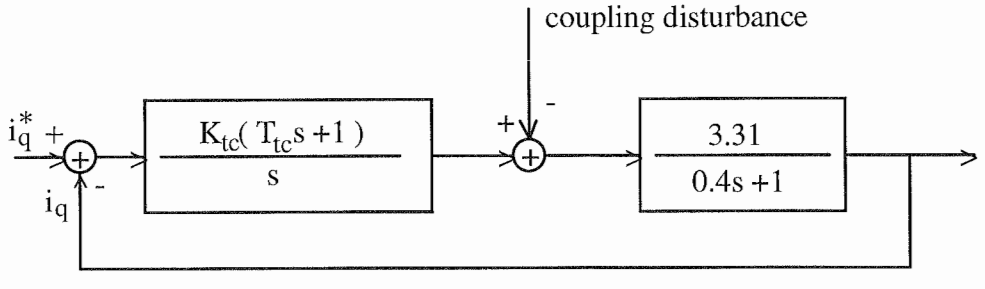


Fig 3.4, Torque current loop

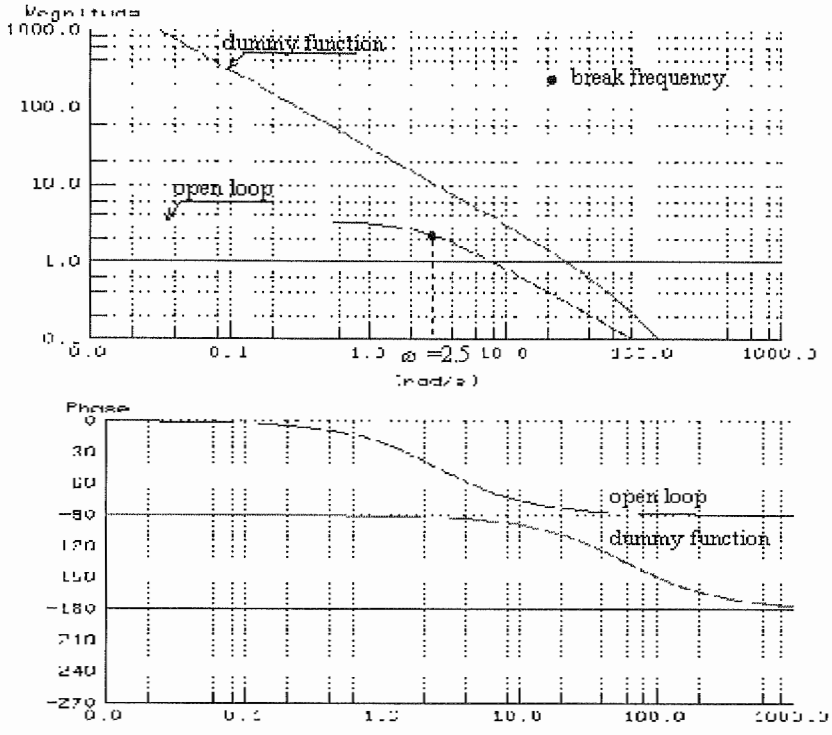


Fig 3.5, Bode plot diagram of the torque current open loop

The Bode plot diagram of the Dummy function Hd and the torque current loop are shown in fig 3.5. Obviously, the dynamic of torque current open loop is much slower than expected (10 Hz compares with 60 Hz).
When a PI controller is added, the Bode plot diagram of the open loop function will be shifted to the Bode plot of the dummy function. To estimate the parameters of PI control, the gain K_{tc} is first chosen depending on the specification of error due to decoupling voltage disturbance and is limited by the maximum value :

$$K_{tc-max} = \frac{32}{3.3} \approx 10 \qquad (3.12)$$

Then, the time constant T_{tc} is determined so that the Bode plot of the open loop including the controller coincides with the Bode plot of the dummy function. If the gain of the PI controller is chosen equal to the maximum value $K_{tc-max} = 10$, time constant will be $T_{tc} = 0.4$s.
Fig 3.6 shows the Bode plot diagram of the torque current loop with the PI controller and fig 3.7 shows the closed loop unit response. The unit response quite satisfies the specifications, ie it reaches the peak value at tp = 0.1s without overshoot. This is explained by the fact that the PI controller completely compensate for the time constant of torque current open loop and therefore the closed loop behaves like a first order system.
By adding the PI controller, the torque current open loop also improves the steady-state accuracy of the system and reduces the sensitivity to motion induced coupling voltages.

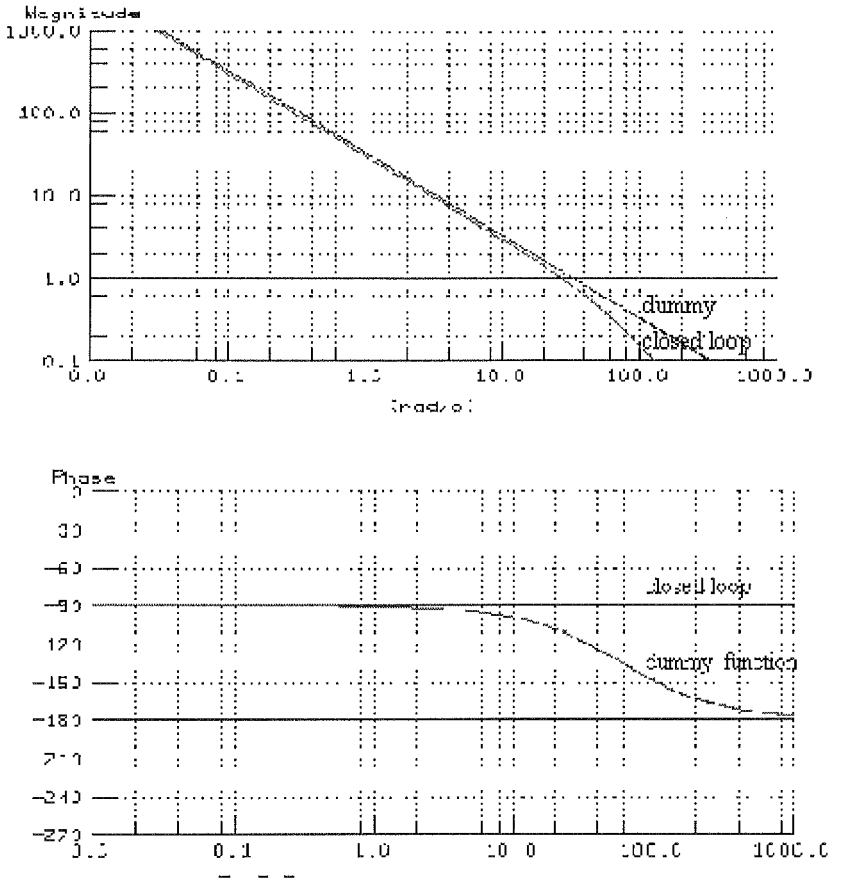


Fig 3.6, Bode plot diagram of the closed loop torque current

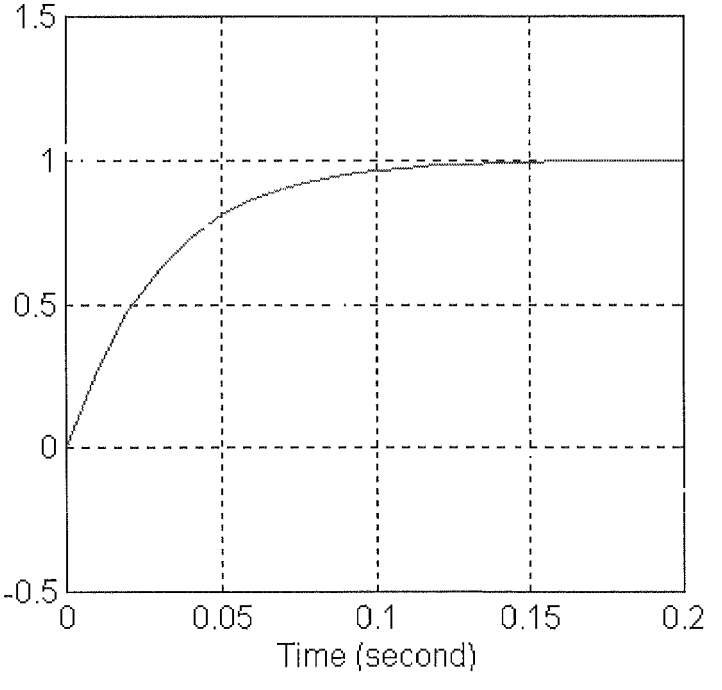


Fig 3.7, Unit response of the closed loop torque current.

3-3-3, Magnetising current loop:

As discussion shown above, the proposed method to synthesise PWM-IM vector control system suggests that the motion induced coupling voltages can be considered as the disturbance to reference voltage. Therefore, the both the torque and magnetising current loops are decoupled and can be designed as a linear systems.
Fig 3.8 shows the block diagram of the magnetising current loop.

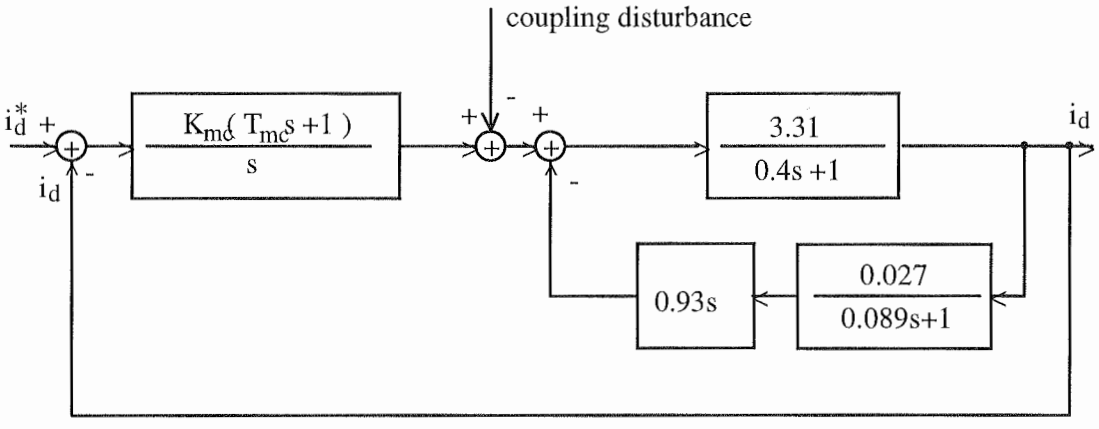


Fig 3.8, Block diagram of the magnetising current

The transfer function of the magnetising current open loop is derived from fig 3.3 (see also appendix B) :

$$H_{mc}(s) = \frac{3.31(0.089s+1)}{(0.4s+1)(0.0885s+1)} \qquad (3.13)$$

Suppose that the specifications of magnetising current loop are similar to that of the torque current loop, ie η = 20% and tp = 0.1s, the dummy function is determined as eq (3.11)
Fig 3.9 shows the Bode plot diagram of the dummy function and the magnetising current open loop.
Using the Bode plot technique , the gain of the PI controller is found K_{mc} = 10 and time constant T_{mc} = 0.4s
Fig 3.10 shows the Bode plot diagram of the torque current loop with the PI controller and fig 3.11 shown unit response closed loop. The unit response quite satisfies the specifics, ie it reaches the maximum value at tp = 0.1s without overshoot. This is explained that the PI controller completely compensate for the time constant of torque current open loop and therefore the closed loop acts as first order system.
By adding the PI controller, the torque current open loop also improves the steady-state accuracy of the system and reduces the sensitivity to motion induced coupling voltage.

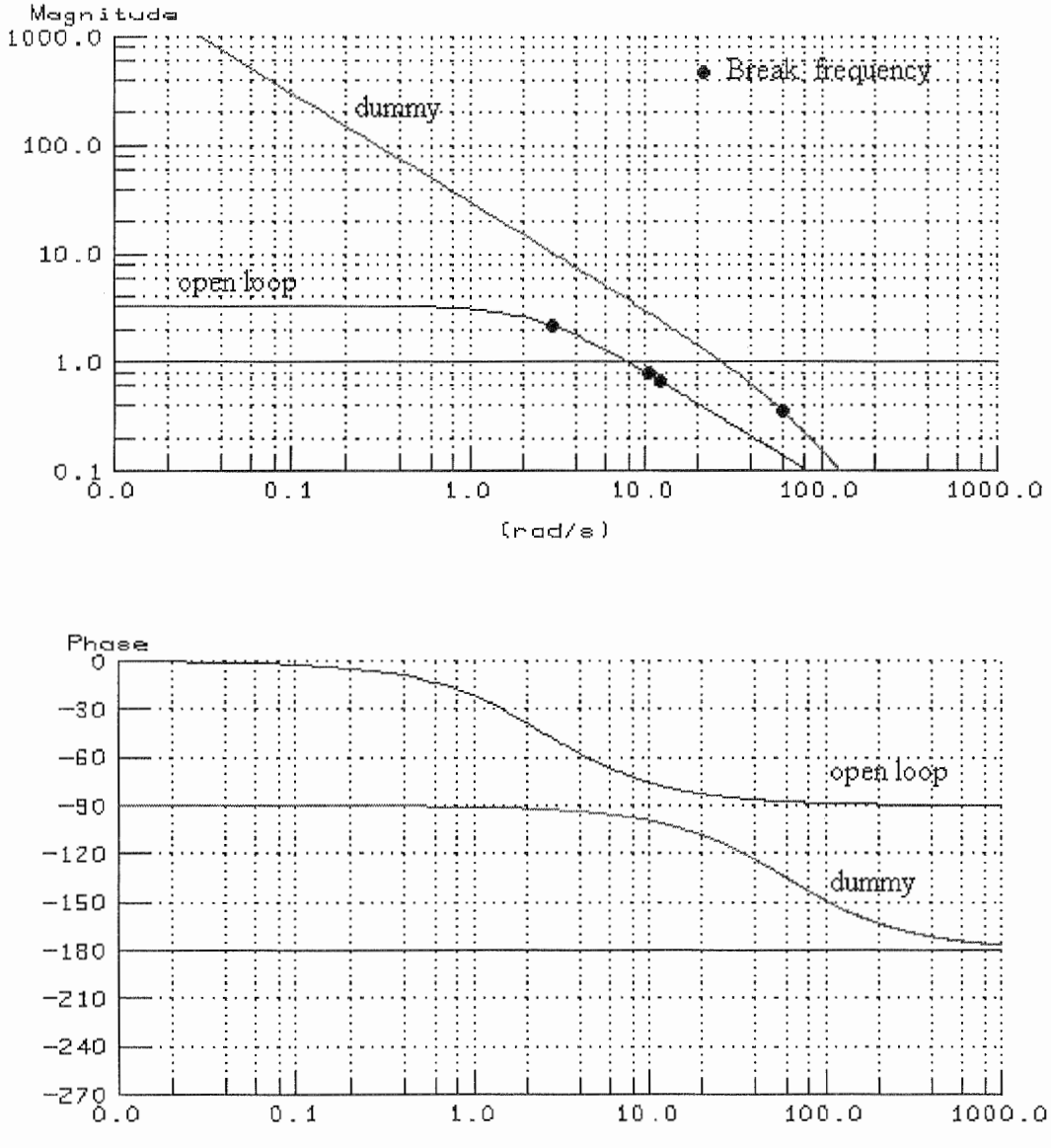


Fig 3.9, Bode diagram of magnetising current-open loop.

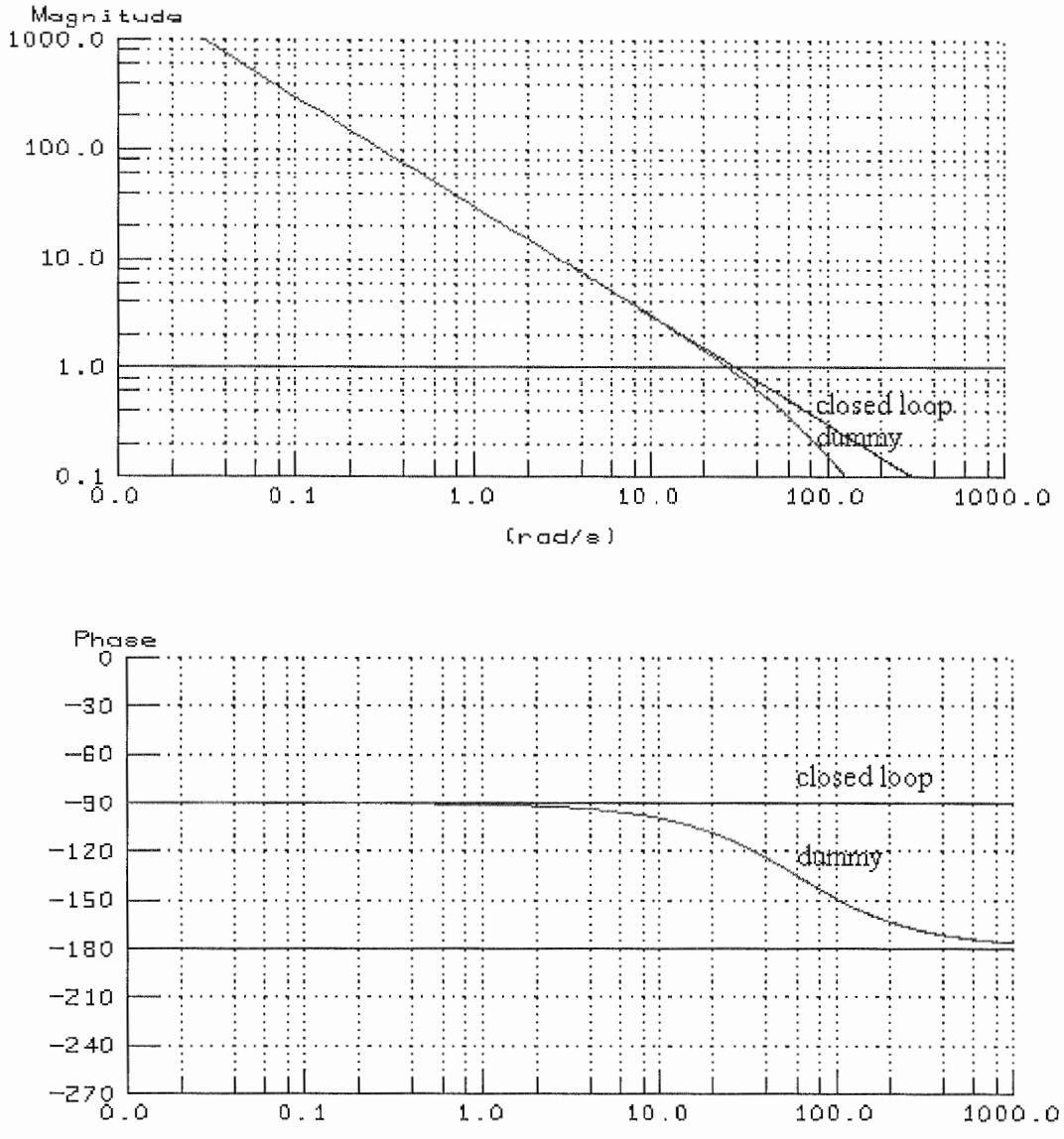


Fig 3.10, Bode diagram of magnetising current-closed loop

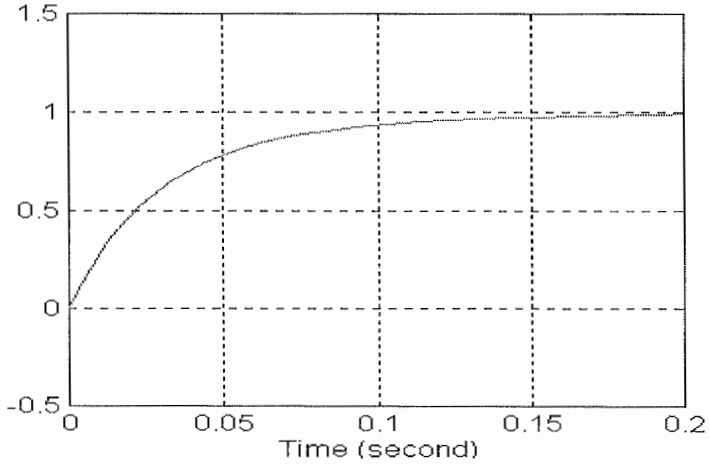


fig 3.11, Unit response of magnetising current loop

3-2-4, Speed loop :

Suppose that overshoot η of the speed loop is required less than 10% and peak time is within 0.2s. The dummy function for the speed loop can be obtained from(3.14) (appendix B).

$$H_s(s) = \frac{19.5}{s(0.043s+1)} \qquad (3.14)$$

The block diagram of the speed loop is :

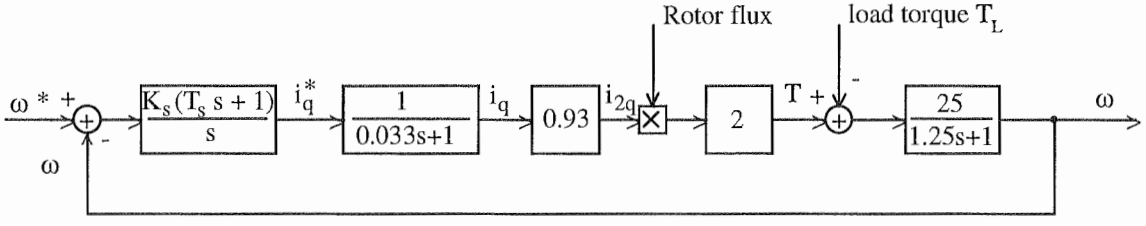


Fig 3.12, Block diagram of the speed loop.

It can be seen that the speed loop still contains a non linear block. That is the multiplier between the rotor flux and rotor current to produce the motor torque. However, this problem can be overcome if the nonlinear multiplier block is considered as a variable amplifier. Because the rotor flux is constant ψ = 0.3 Wb when motor is controlled below the rated frequency and deceased up to 0.1 Wb when motor is controlled above rated frequency, the range of the variable amplifier gain is 0.1÷0.3. By such a way, the gain of the PI speed controller could change from 0.93 to 2.8. Fig 3.13 shows the rang of Bode plot of closed loop system when the gain of the variable amplifier change from 0.93 to 2.8 in which the time constant of the PI speed controller is chosen Ts = 1.25 in order to compensate for the mechanic time constant of the motor.

Fig 3.14 shows the Bode plot of the closed loop at the gain Ks = 1.25. In this case, the speed response is faster than that obtained from dummy function. However, when the motor speed increases, the motor flux decreases. This decrease gain of speed loop. The response will be slower but still kept within specifications.

Fig 3.15 and 3.16 shows the unit response of speed loop at low speed ψ = 0.3 Wb and at high speed ψ = 0.1 Wb. As mentioned above, the decrease of motor torque has large influence on the dynamic response. But system still satisfies specific requirements : overshoot is less than 10% at low speed and peak time is within 0.2s at high speed.

As a last step in control design, whole system is simulated by MATLAB program at most important points of speed range. That are at low speed with no load and full load, and at high speed with no load and full load. Then the parameters of controllers are tuned until system reaches desired dynamic performance for all theses points. Fig 3.17 through 3.20 depict the dynamic response of the motor speed and current as well as flux at these points with a small change in the gain of the current controllers. Therefore, the last set of parameters of the controllers are chosen as :

Ks = 1.2 ; Ktc =12.5 ; Kmc =12.5 ;
Ts = 1.25 ; Ttc = 0.4 ; Tmc = 0.4 ;

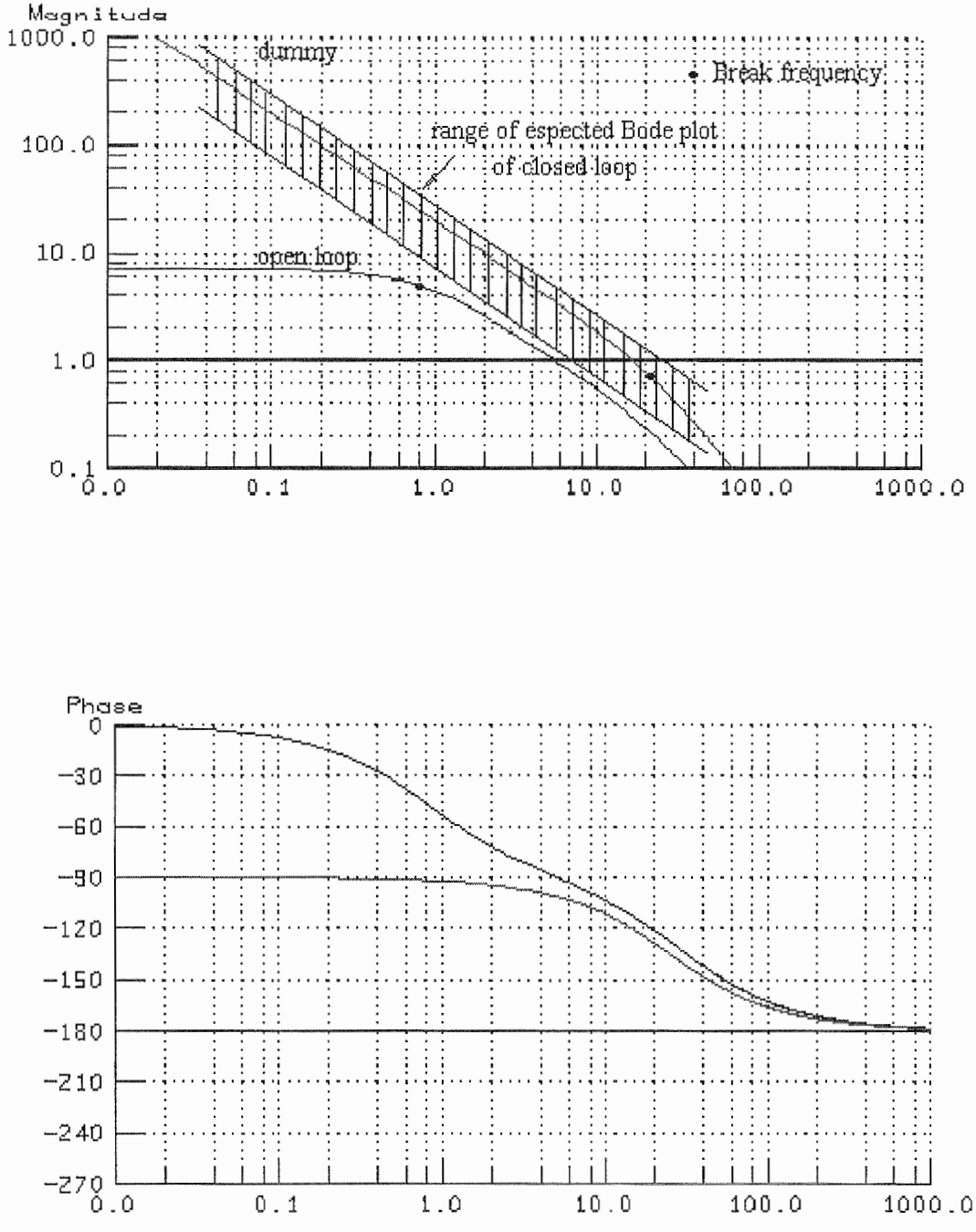
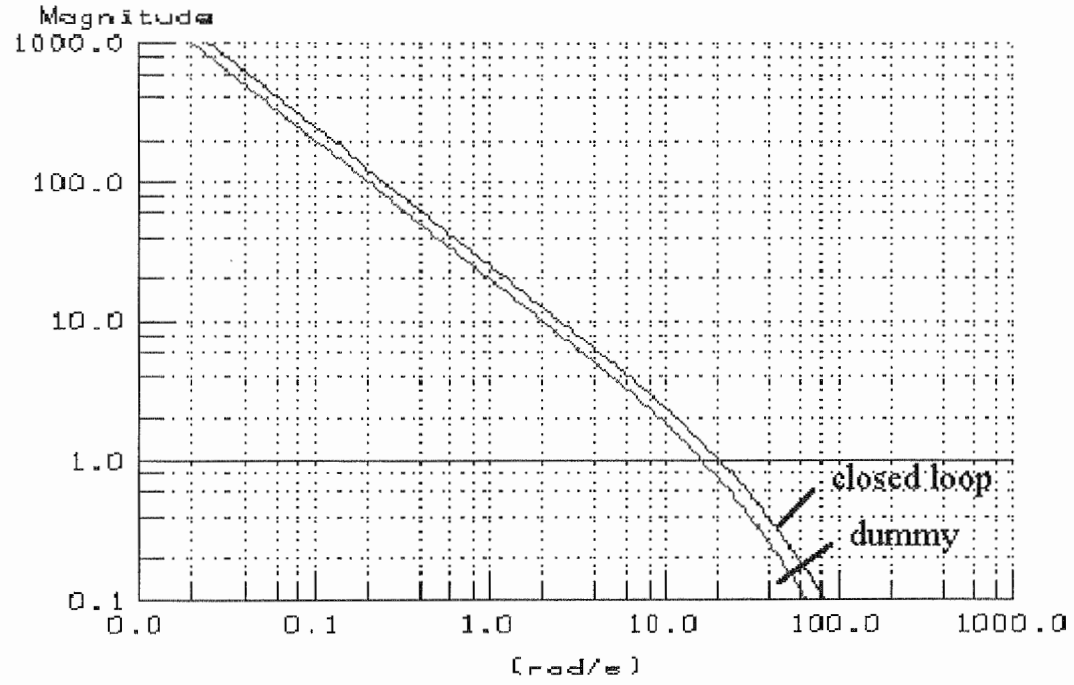


Fig 3.13, Bode plot of speed- open loop.



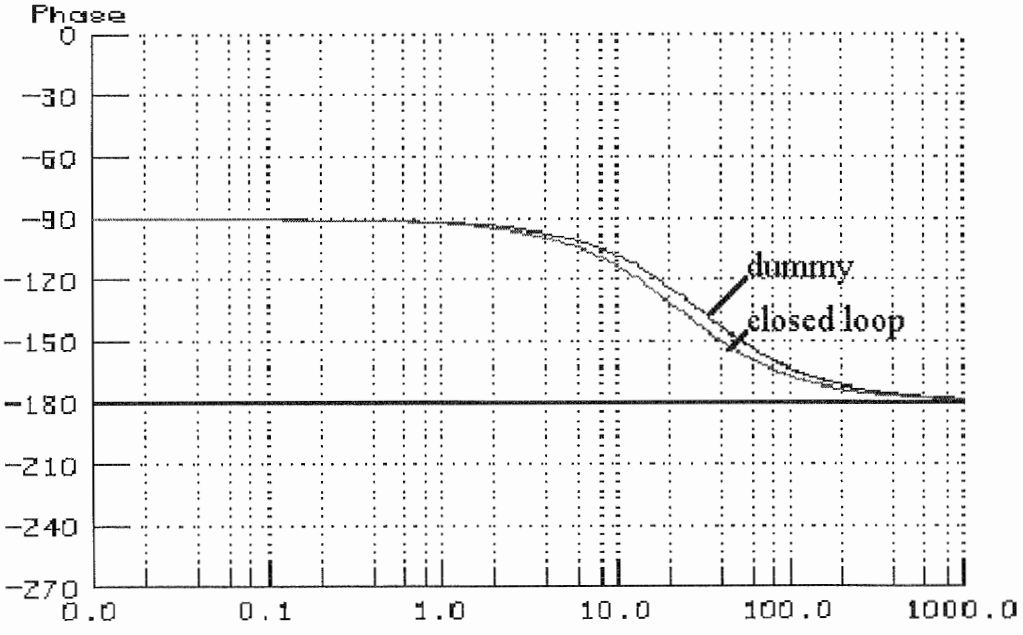


Fig 3.14, Bode plot of speed- closed loop.

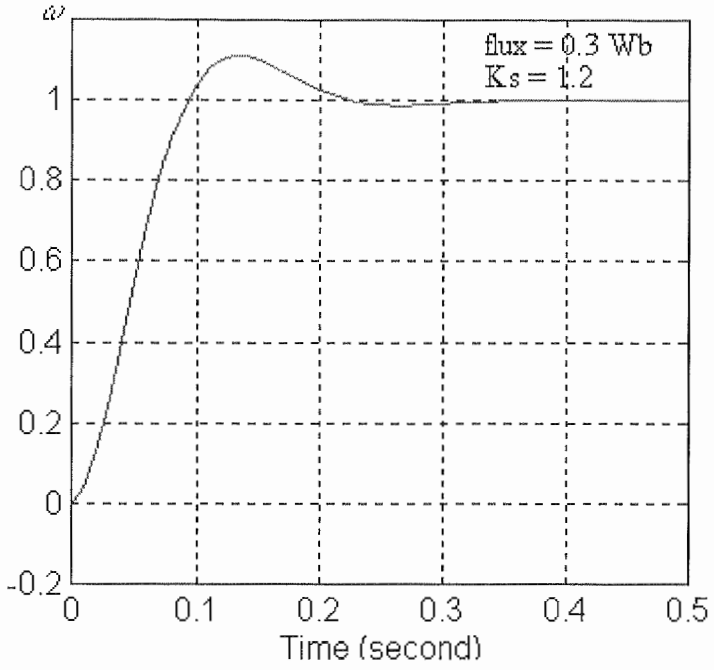


Fig 3.15, Unit respond of system at low speed, $\psi = 0.3$ Wb.

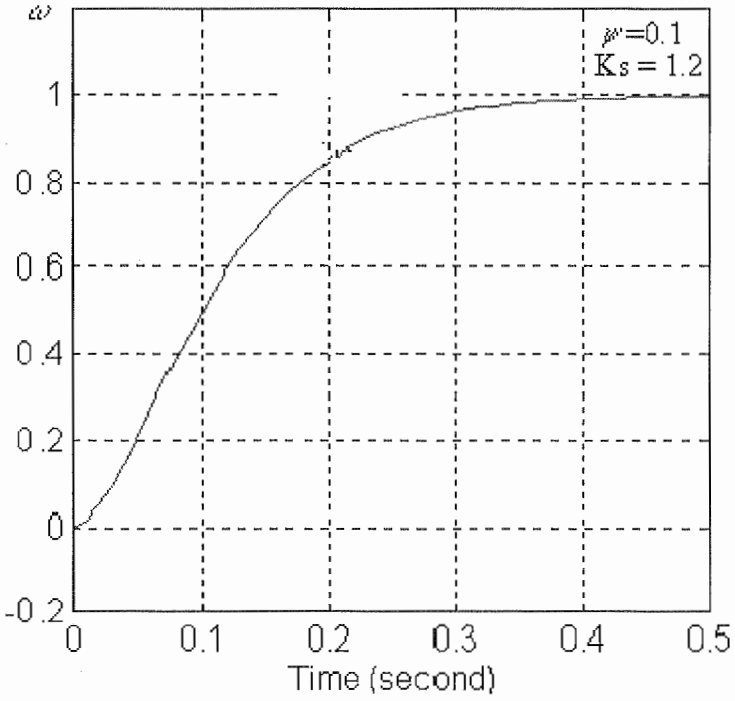


Fig 3.16, Unit response of system at high speed, $\psi = 0.1$ Wb.

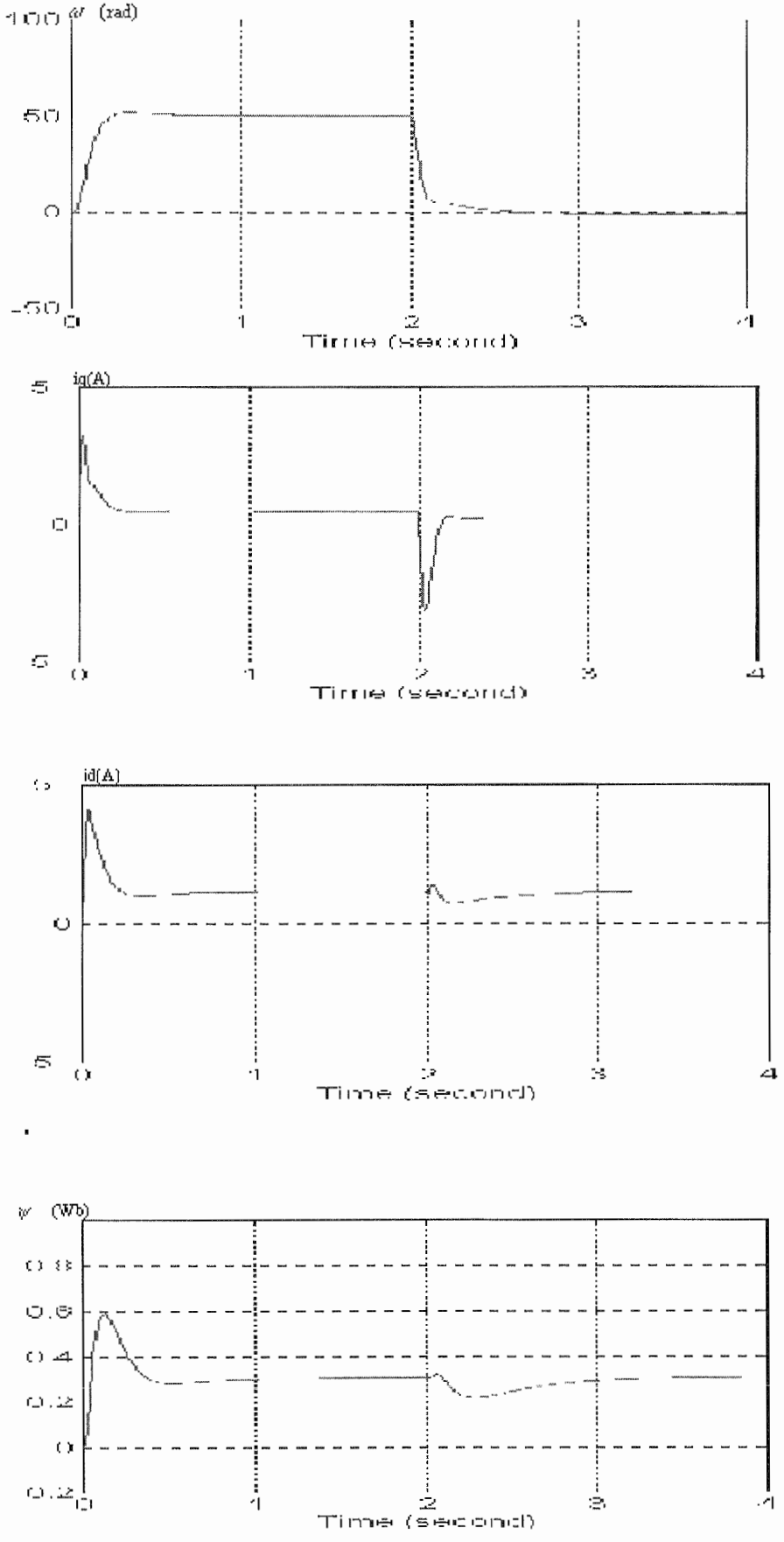


Fig 3.17, Dynamic response of system at low speed and no load.

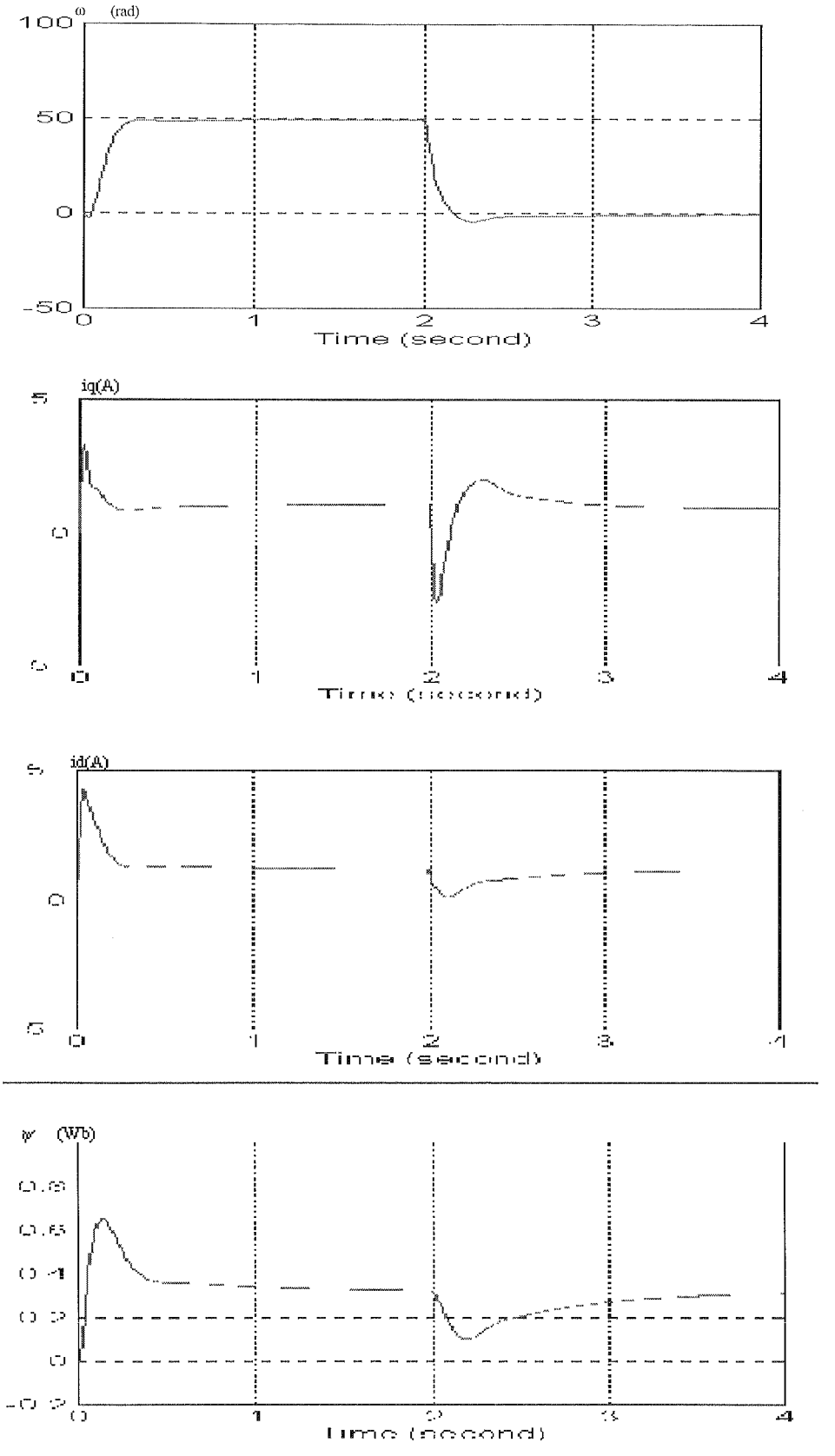


Fig 3.18, Dynamic response of the system at low speed, full load

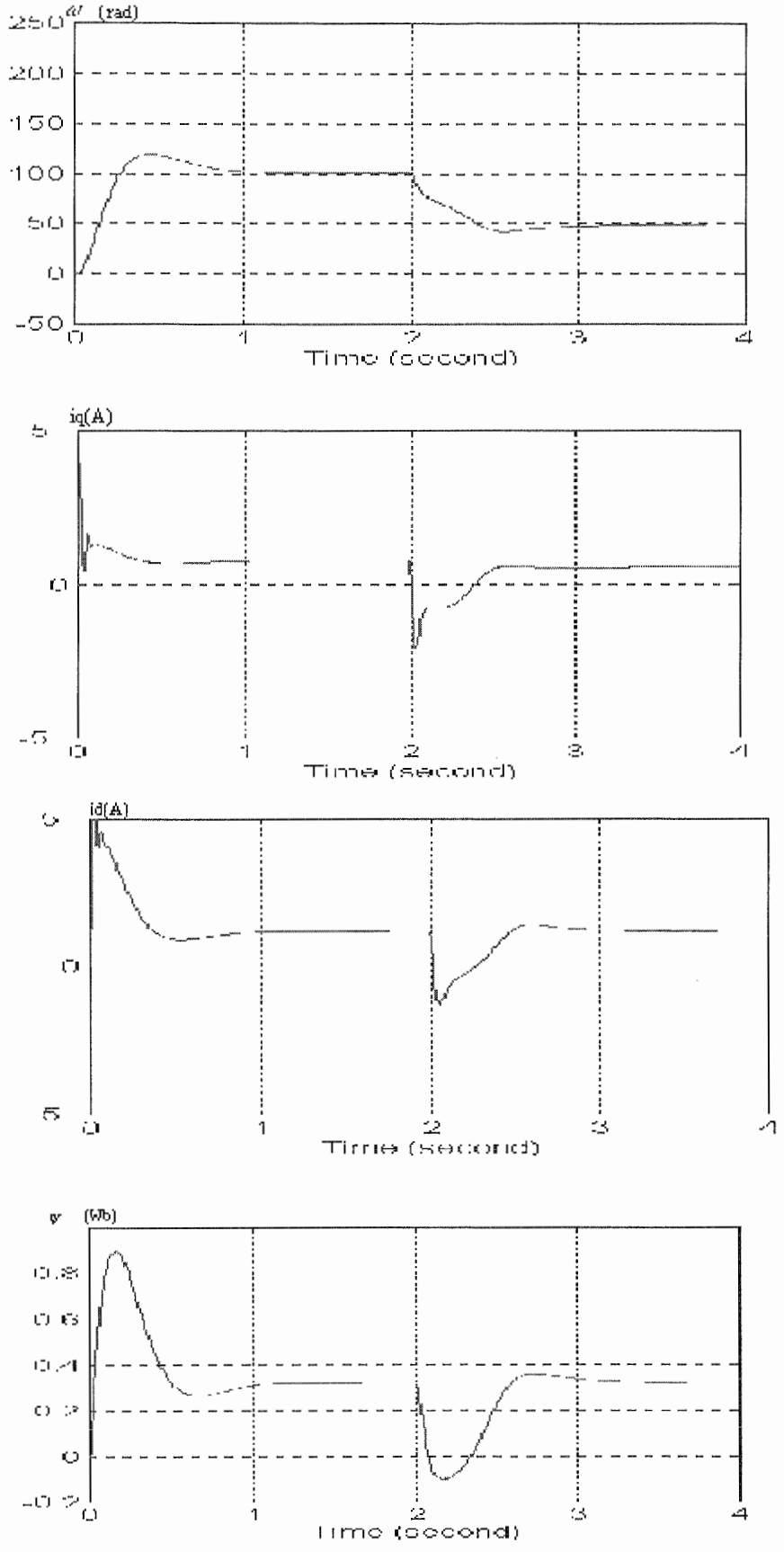


Fig 3.19, Dynamic response of system at high speed, noload

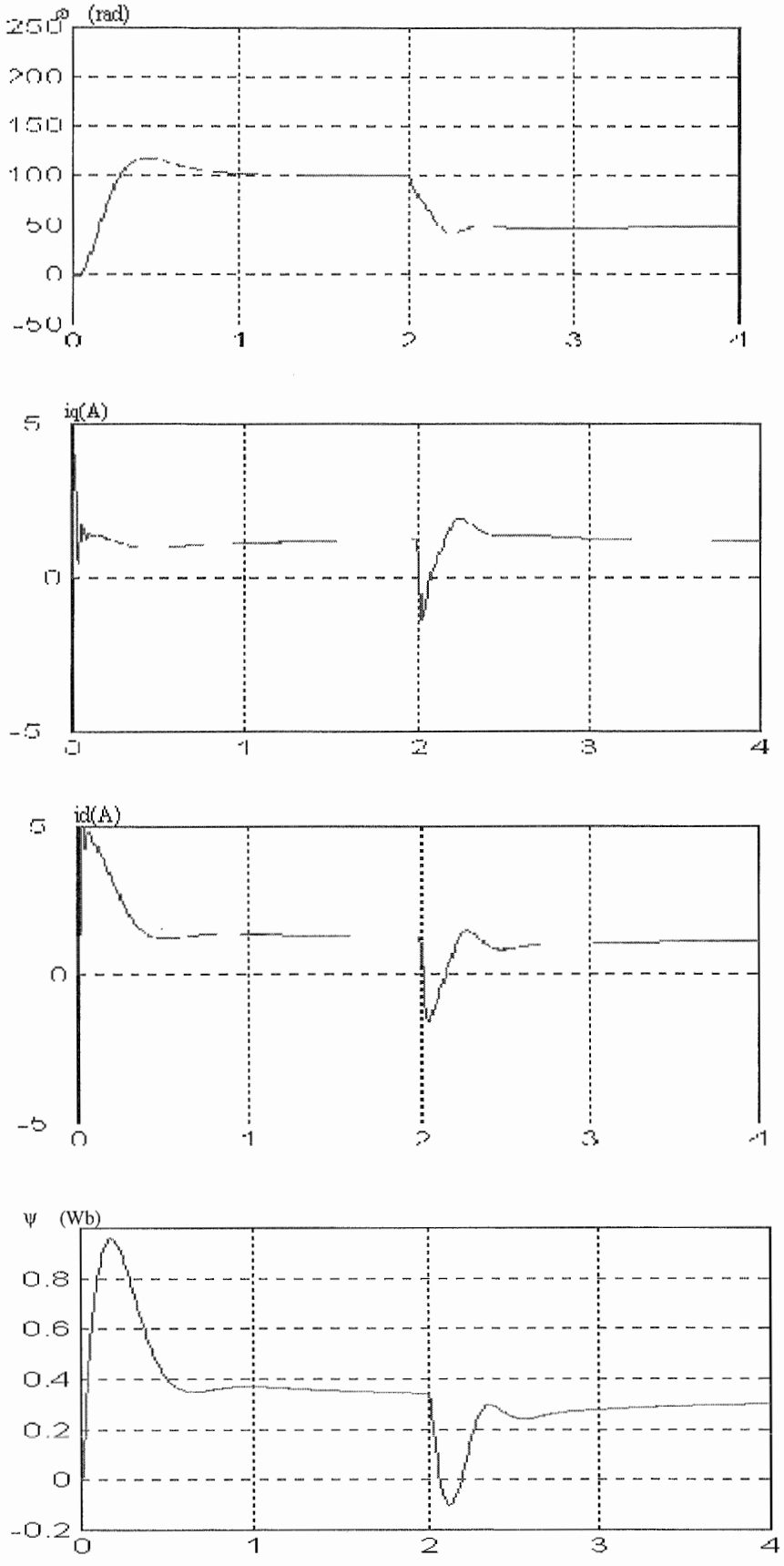


Fig 3.20, Dynamic response of system at high speed, full load.

3-4, Effects of digital implementation.

As mentioned at the beginning of this chapter, this project employs an indirect control procedure that totally ignores the effects of the sampler and digital computer on the real time system. Therefore, this chapter will remain incomplete without some discussion of these effects on the dynamic response and steady sate error of the system.
studies in [14] shows that there are two main factors that could influence on digital system: the sampling rate and quantisation error.

3-4-1, Sample rate:

+ Choice of sample rate :
The selection of the best sample rates for a digital control system is a compromise. Generally, the performance of a digital control system improves with increasing sample rate, but cost may also increase with faster sampling. A decrease in sample rate means more time is available for the control calculation; hence, slower microcomputer are possible for a give function, or more control capability is available for a given microcomputer. Either result lower cost per function.
For PWM-IM drive system with some A/D converters, slower sampling means less conversion speed is required, which will also lower cost. Furthermore, it can be seen that faster sampling require a large word size, which would also increase cost.
All these arguments suggest that the best choice is the lowest sample rate that meets all performance specification.
+ Sampling theory :
The sampling theory [14] states that in order to reconstruct an unknown band-limited continuous signal from samples of that signal, the sample rate must be at least twice as fast as the highest frequency contained in that unknown signal. This theory applies to closed-loop PWM-IM drive system because reference motor speed ω is considered as unknown signal that must be followed by the motor speed. Based on the sampling theory, the sample rate must be at least twice the required closed-loop bandwidth of that system, that is 40 Hz for speed loop and 120 Hz for current loops.
If the sample rate is chosen lower than these limitation, the system would unstable or considerable slower than specification.
+ Time response and smoothness:
The sample rate 40 Hz for speed loop and 120 Hz for currents loops provide the fundamental lower bound of the sample rate. In practice, however, these lower bounds would be judged far too slow for an acceptable time response. Therefore, It would be typical to chose a sample rate at 10 to 40 time of closed-loop bandwidth in order to limit the magnitude of the control steps. This means that the desired sample rate for a reasonable smooth time response for speed loop is 200 to 8000 Hz and current loops is 600 to 2400 Hz.
+ Command change delay :
In addition to the smoothness issue, it is important to reduce the delay between a command change and the system response to that command change. A command motor speed input can occur at any time through a sample period; therefore, there can be a delay up to full sample period before the controllers are aware of this change.
For a system with human input such as IM drive system, the sample rate should be at least 20 time band width frequency in order to kept command delay time to be less than 10% of rise time.

+ Multirate sampling :
It is useful to use different sample rate on the speed loop and current loops. By such a way, the system is called multirate (MR) system in which current loops (inner loops) are normally faster than speed loop (outer loop).
The sample rate selection for multirate system is also carried out using discussion showed above. However, care should be taken in order to avoid an unacceptable movement of the inner roots [14/p508].

3-4-2, Quantisation effects :
The fixed point is normally used to represent a number in digital calculation. Therefore, a number has to be quantised by either truncation or rounding process. It result in errors known as quantisation errors.
Quantisation errors can have a detrimental effects on system performance at fast sample rate with a word size less than 10 bits. Therefore, it would be useful to analysis the system's sensitivity to quantisation errors and possibly to limit the sample rate to reduce sensitivity. Offcourse, another approach that can reduce the effects of quantisation errors is use of microcomputer with higher word size bits. Practically, the quantisation error is typically not an issue by using microcomputer with 16 or more bits.

As conclusion, this chapter discusses the dynamic of the PWM-IM transvertor control system. A model of system in the form of space-state vector is derived. A new method which employs the advantages of software simulink tool is introduced to determine parameter of controllers. Simulation of whole system shows that the couple induced voltages between d and q axis of motor influence strongly on performance of system and these effects change with change of the operation point of system. By tuning the set of parameters of controllers at most important points, the best set of control parameters can be chosen so that the worst-case system performance is acceptable. Finally, the effects of digital implementation is discussed. It expressed that the best sampling policy for system is a complicated matter involving compromise a mong many factors. Therefore, the analysis of sample rate tools to make the most cost-effective choice are described.

Chapter 4 : Variable-voltage variable-Frequency PWM modulator.

A requirement for an IM speed control by the use of a variable-frequency variable voltage source is that the wave form contains the lowest possible harmonic content. The best solution would be a voltage source inverter that generated sinusoidal wave forms. Such a device would be elaborate and expensive since it would requires a large number of switching element.
For modest speed range, a six-step technique with variable voltage dc supply can meet the requirements. However, as the speed becomes large due to a drive requirement for low and very low speed operation, some problems become significant. First, the supply voltage becomes so low as to impair the commutation capability of the inverter. Second, harmonics of the six-step wave form interacts with the fundamental to produce low frequency torque which cause irregular rotation at very low speed. All these problem can be overcome by the use of the PWM technique.
There are many advantages of the PWM technique comparing with the six-step technique. The ideal requirements of sinusoidal voltage can be closely approximated by the synthesis of voltage waveform using PWM technique. Because the fundamental component of PWM can be controlled, the harmonic content can be made low and the harmonic order is higher than that obtained with six-step technique. Nowadays, PWM technique is widely used to perform variable voltage frequency source.
There are a number of schemes of PWM, prominent among these are sinusoidal PWM [1,2,3], PWM with uniform sampling [5], selective harmonics elimination[2,5], efficiency optimal control [10/p375],[16] and so on.
This project employs sinusoidal PWM technique because of its simply in implementation.

4-1, Low frequency PWM :
4-1-1, Natural sampling technique:
a) asynchronous control :

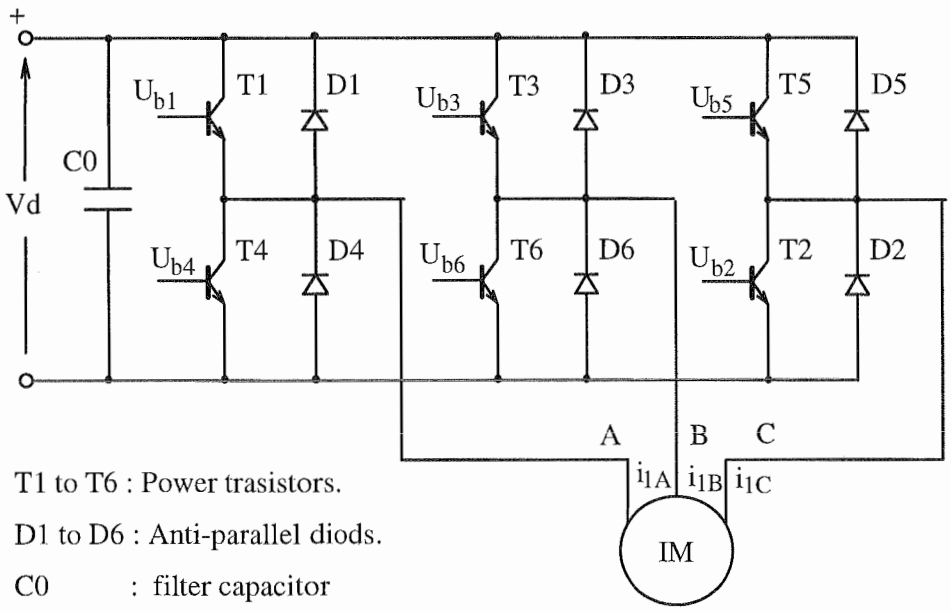


Fig 4.1, Inverter circuit.

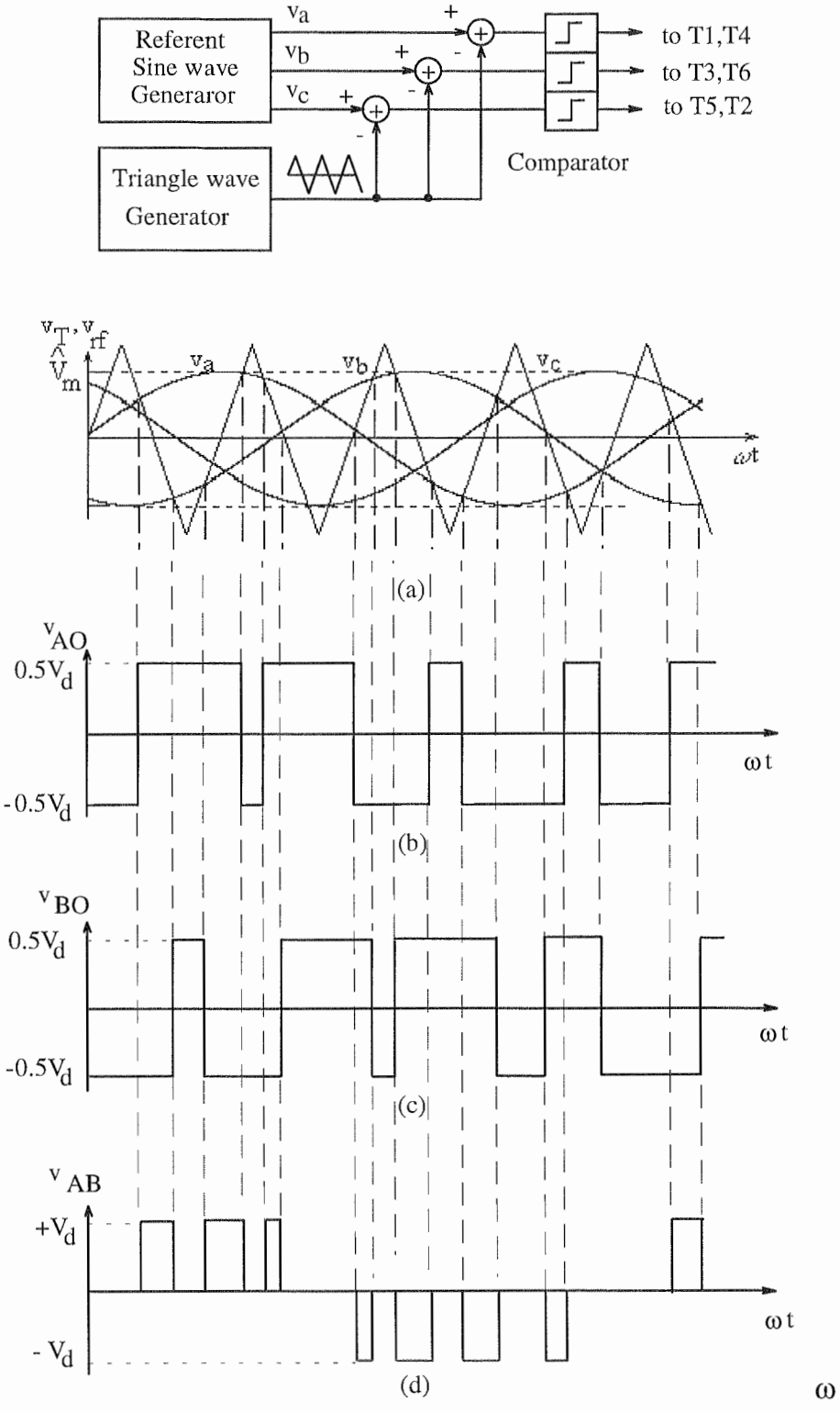


Fig 4.2, Principle of the sinusoidal PWM

Fig 4.1 shows the inverter circuit and fig 4.2 shows the principle of sinusoidal PWM to control IM below the rated frequency. It can be explained as follow :

+ Three phase reference voltage $v_a(t), v_b(t)$ and $v_c(t)$ are compared in three separate comparator with a common triangular carrier wave $v_t(t)$ (fig 4.2). The intersection of

the reference voltage and carrier signal determine both the onset and duration of the modulated pulse and hence the pulse pattern. The circuitry actuating the turn-on and turn-off of the transistor inverter is controlled by sensing these intersections.

+ To calculate $v_{AB}(t)$, let consider the operation of switch pairs (T1,T4) and (T3,T6) :

- T1,T4 : T1 is on when $v_a(t) > v_t(t)$.
  T4 is on when $v_a(t) < v_t(t)$.
  This produces phase voltage $v_{AO}(t)$ as fig 4.2 (b).
- T3,T6 : T3 is on when $v_b(t) > v_t(t)$.
  T6 is on when $v_b(t) < v_t(t)$.
  This produces phase voltage $v_{BO}(t)$ as fig 4.2 (c).
- Line Voltage :
  $v_{AB}(t) = v_{AO}(t) - v_{BO}(t)$ as fig 4.2 (d).

+ If m is module index :

$$m = \frac{v_m}{v_T} \tag{4.1}$$

and p is frequency module index :

$$p = \frac{f_c}{f_1} \tag{4.2}$$

where fc = carrier frequency.
f1 = reference frequency.

reference [2/p299] shows that for $m \leq 1$, the fundamental component in the phase voltage waveform $v_{AO}(t)$ is given by :

$$v_{AO1}(t) = \sqrt{2} V_{AO1} \sin\omega_1 t$$

$$V_{AO1} = \frac{m V_d}{2\sqrt{2}} \tag{4.3}$$

For m > 1 (known as overmodulaton), the relationship between $v_{AO1}(t)$ and module index m is no longer linear.

For m >> 1, PWM reaches six step mode and the fundamental component of V_{AO1} reaches the maximum value :

$$V_{AO1\text{-}max} = \frac{\sqrt{2} V_d}{\pi} \tag{4.4}$$

From Eq (2.29), the amplitude of $v_{AO1}(t)$ can be controlled by changing modulation index m, ie by changing V_m if V_T is fixed, and the frequency of $v_{AO1}(t)$ can be controlled by changing frequency of the reference waveform. Obviously, the frequency index p should be large to reduce the effects of harmonics. However, the maximum value of p is limited by switch capability of power devices.

b) synchronous control :

At asynchronous control shown above, the variable frequency variable amplitude sine wave is compared with a triangular waveform of fixed frequency. In this case, the carrier waveform is asynchronous with modulating wave. The quantity of the output waveform will depend on the modulating index m. The highest this ratio, the highest will be the frequency of the unwanted harmonics in the output waveform, and the ripple current that is produced in an inductive load such as IM will be less. The draw back to this waveform generation method is that the carrier and modulating frequency are generally incommensurable so that the PWM wave is non-periodic and therefore contain components of lower frequency than wanted frequency component (sub-harmonics). The flux produced by the subharmonics may be considerable and can seriously interfere with the efficient operation of the IM.

The speed of currently available BJT's and MOSFET's and the losses associated with the switching of these devices have made the higher carrier to modulating frequency impractical. It has thus been necessary to devise other way of avoiding the generation of the subharmonics in the output waveform. One way this can be achieved is by synchronising the carrier and modulating wave so that the carrier frequency is an integer multiple of the modulation frequency. A more detailed analysis indicates that the frequencies of the reference and carrier wave should satisfy the following relation :

$$f_c = 6nf_1 \qquad n \geq 1 \qquad (4.5)$$

The PWM waveform is than periodic and contains only harmonics which are integer multiple of fundamental.

The difficulties with synchronous operation is that the carrier and modulating wave are synchronised . Therefore, the carrier frequency must vary over wide range as the output frequency. However, it is not usually practical to allow the carrier frequency to vary so widely, since, if it is too low, the motor time constant is insufficient for adequate smoothing of the motor current, and if it is too high, the inverter commutation losses are unacceptably large.

To overcome this problem, the modulating index is changed at interval throughout the operating range of the motor speed in order to keep the carrier frequency within prescribed limit. This method is known as sliding mode and will be discussed in more detail at the end of this chapter.

2-1-2, Uniform sampling technique

The natural sampling technique of the sinusoidal PWM has found wide acceptance for controlling electronic switching power inverter. PWM control signals were originally generated with the help of electronic hardware, but lately, microcomputer has begun to play an important role in the design of control signal generator for power inverters gradually assuming more and more functions.

The microcontroller-based PWM have been developed principally on the basis of the look-up table. In the natural sampling technique, the number of notch angles for a wave pattern tends to increase at lower fundamental frequency and the number of wave patterns stored tends to be limited. Even if the memory size is considered to be no constraint, the hardware and software designs of the present modulator are such they often do not provide good angle resolution, and the output wave do not respond adequately in real time with change in voltage and frequency commands. Although

some attempts have been made to implement the low frequency region by the computation intensive natural sampling method, this have met with limit success.
[11] describes a sampling technique, known as uniform sampling. Using the uniform sampling technique, PWM can be easily implemented on microcontroller by hybriding the computation intensive and look-up table method.

a) Principle of the uniform sampling technique :
The principle of the uniform sampling technique is explained in fig 4.3,.

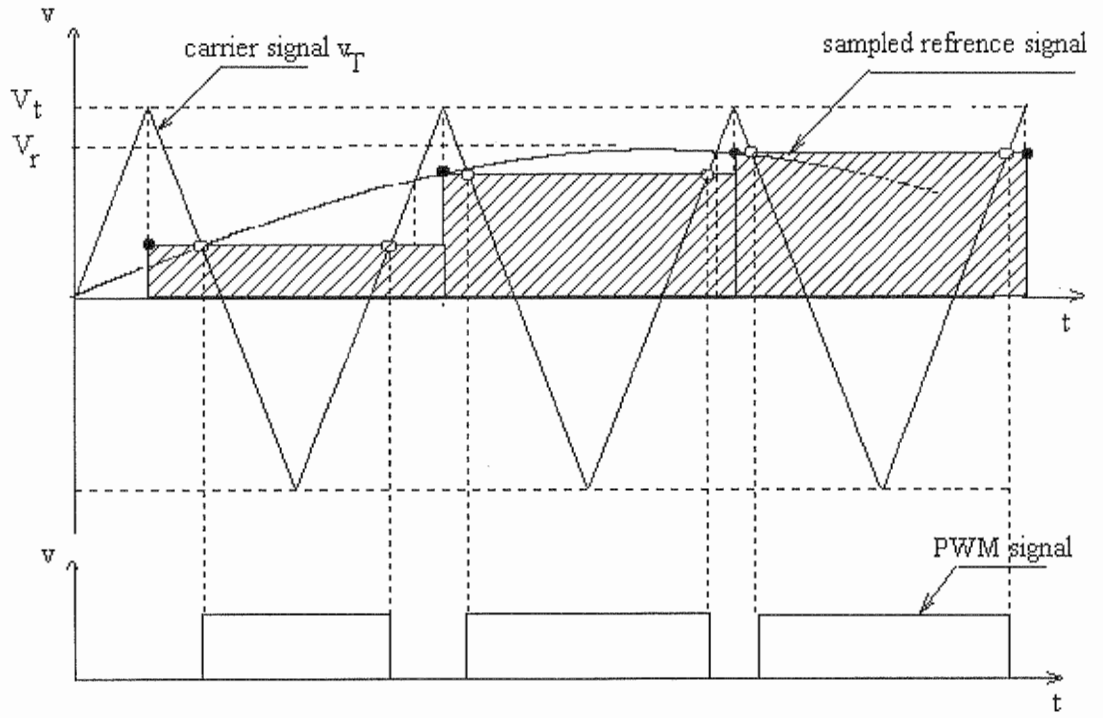


Fig 4.3, Principle of uniform sampling technique.

As shown in previous section, in the natural sampling method, the carrier wave is compared directly with the reference wave to determine the switching instants, ie, it is a process of intrinsic natural selection of the sampling points. In the uniform sampling technique, which is based on the sample-and-hold principle, the reference wave is sampled at sampling frequency Fs. Furthermore, the sampling frequency Fs is chosen equal to the carrier frequency fc. the sampled reference wave is then compared with the carrier wave to produce PWM signals. By that way, PWM in the uniform sampling technique is always symmetrical as shown and therefore it can be pre-calculated by microcomputer.
The uniform sampling technique has been extensively evaluated and shows significant improvement in low frequency harmonics and limitation of the subharmonic problem at non-integer ratios. However, most advantage of the uniform sampling technique is that it can be easily adaptable to microcontroller implementation.

b) Uniform sampling PWM implementation :

Using uniform sampling technique, a PWM can be implemented with help of the microcontroller as shown in fig 4.4.

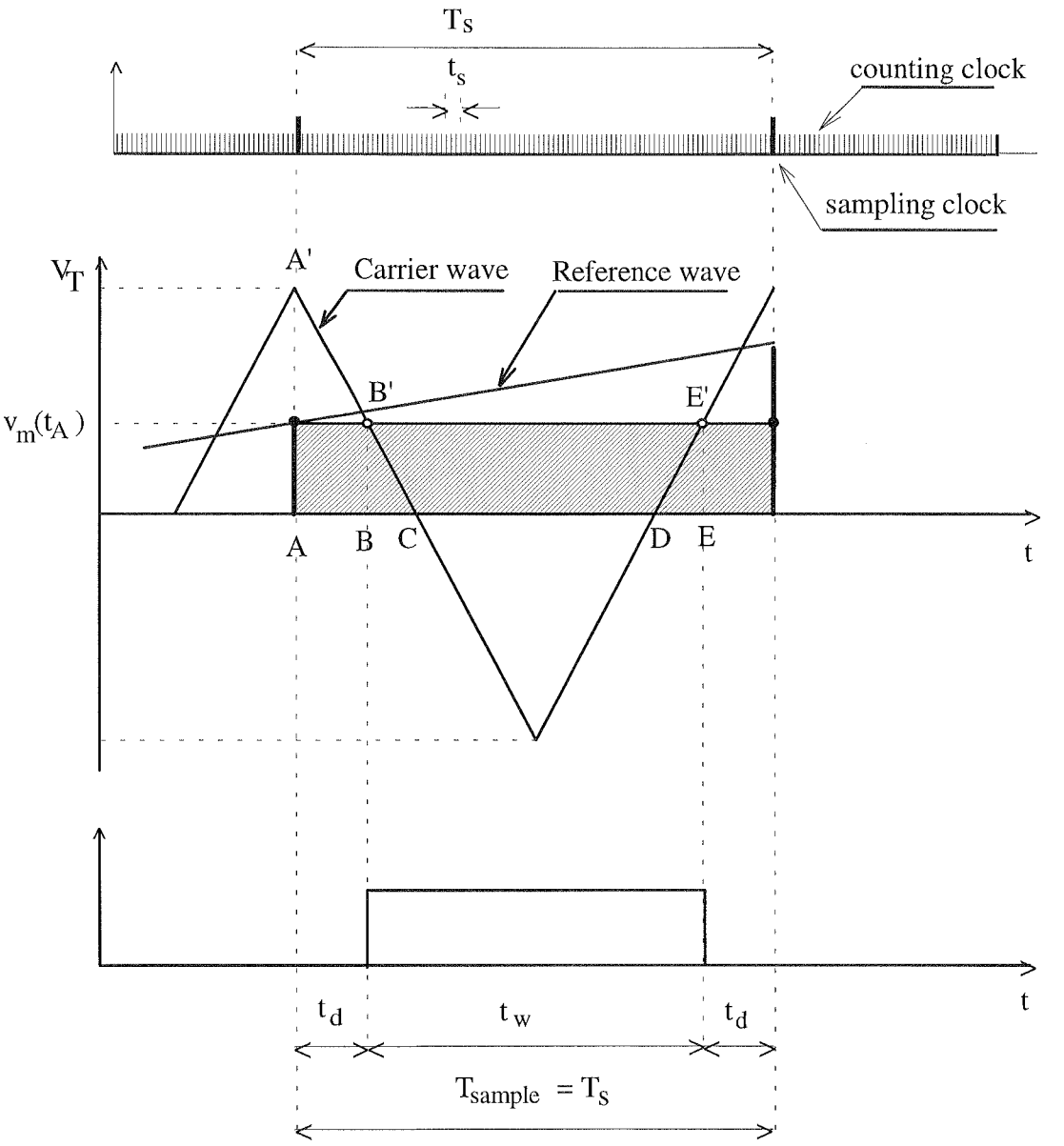


Fig 4.4, Microcomputer based PWM implementation principle.

The microcomputer memorised number of amplitudes of 1-pu quarter-cycle sampled reference wave at equal angular interval as shown. Because of 120 phase shift between the phases and the quarter-cycle symmetry for a sine reference wave, the amplitude information for three phase PWM output can be obtained by appropriate locating the address pointers. The 1-pu samples of the reference wave are shown to correspond with the troughs of an equilateral triangle wave of period Tc, ie, Ts = Tc, as characteristics to uniform sampling principle. In actual operation, the microcomputer periodically samples the voltage command , multiple with the 1-pu sample amplitude at that instant, and then generate a symmetrical pulse width as shown

Fig 4.4 shows operation of PWM modulator principle within only one sample reference wave v_m. Here :

Ts = sample interval of reference wave.
ts = basic clock pulse.
td = delay time of PWM.
tw = pulse width time.

The clock pulse with frequency fs=1/ts can be created by a programmable counter. There are two problem concerning with clock pulse counter fs:

1, frequency fs must be large enough to ensure precision synthesis of the PWM wave. In each sample interval Ts, it should be at least 256 pulses.

2, How many pulse required to count sample time Ts, pulse width time tw and delay time td ?

a) Sample time Ts :

$$N_{TS} = \frac{T_s}{t_s} = \frac{f_s}{F_s} = \frac{f_s}{f_c} = \frac{f_s}{af_1} \tag{4.6}$$

where N_{TS} = number of clock pulse to count Ts.

b) Pulse width time tw :

From fig 4.4,

$$BE = 2BC + CD \tag{4.7}$$

Because :

$$BC = \frac{BB'}{AA'} * AC \quad ; \quad AC = \frac{AF}{4} \quad ; \quad CD = \frac{AF}{2}$$

hence :

$$BE = 2\frac{BB'}{AA'} * AC + CD = \frac{AF}{2}(\frac{BB'}{AA'} + 1)$$

or :

$$t_w = \frac{T_s}{4}(\frac{v_r(t_a)}{V_T} + 1) \tag{4.8}$$

$$N_{tw} = 0.5N_{Ts}(\frac{v_r(t_a)}{V_T} + 1) \tag{4.9}$$

where : $v_r(t_a)$ = amplitude of sampled reference at t = t(A)
V_t = maximum amplitude of v_T (15v)
N_{tw} = number of clock pulse required to count tw.

c) Delay time td : From 4.7 , the number of clock count is easily driven :

$$N_{td} = 0.5(N_{Ts} - N_{tw}) \tag{4.10}$$

c, Uniform sampling technique at asynchronous mode :

At low frequency, PWM should operate at asynchronous mode to improve performance as explained in section 4-1-1, The exploded view of part of cycle in this mode is shown in fig 4.5, which is somewhat self-explanatory.

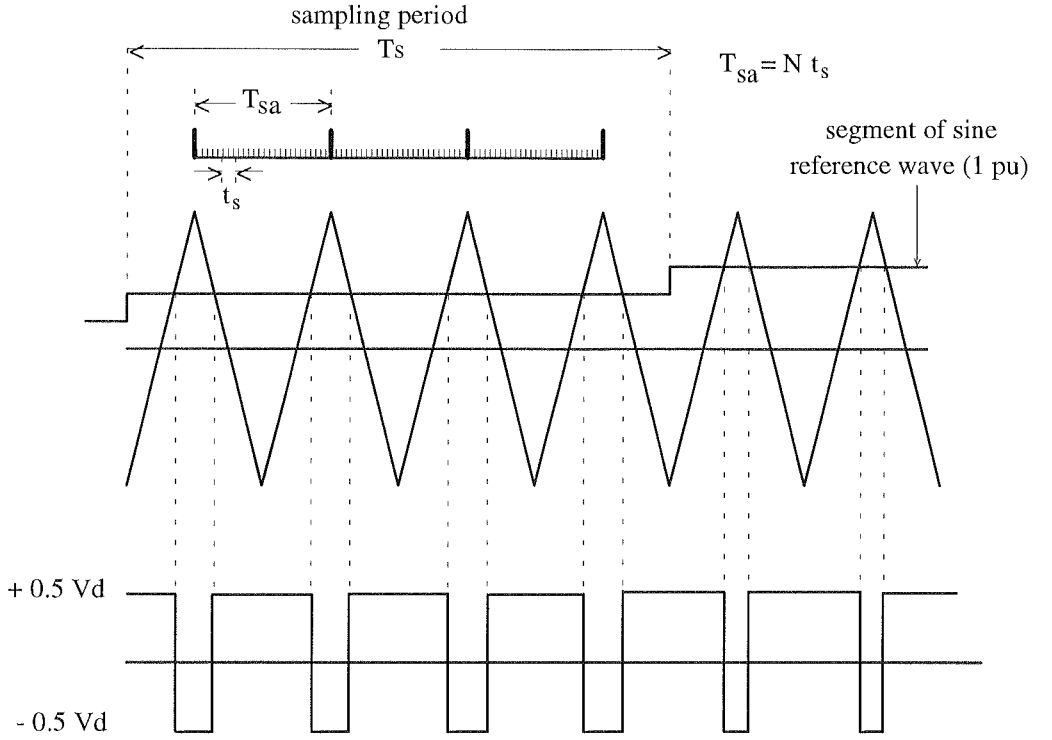


Fig 4.5, Uniform sampling PWM wave generation in asynchronous mode.

The free running frequency deviates from the sampling frequency (Fsa > Fs) because of the limited number of samples available. Here, the reference wave is sampled every Ts period and store into memory buffer. The fixed carrier frequency clock Tsa fetches the sample, multiplies by the mechanism explained before. The counting clock ts is a submultiple of Tsa by the relation Tsa=Nts, where N should be 256. The maximum carrier frequency which determines the number of commutation/s is limited by the switching and commutation losses of the power semiconductor devices. The minimum fundamental frequency is limited by the size of the ts counter.

4-2, High frequency :

At high frequency, uniform sampling technique can not be used because of the timing constraint. Some techniques are studied to solve this problem [27] [33]. Among them, the harmonic eliminate is one of most popular method that is applied inverter with a constant voltage source.

4-2-1, The harmonic elimination technique :

The harmonic eliminate technique is originally based on the notch angle technique. Fig 4.6 shows three basic notch angle : $\alpha 1$, $\alpha 2$ and $\alpha 3$. The principle of the harmonic eliminate is that the angle $\alpha 1$, $\alpha 2$ and $\alpha 3$ are proper choice so that the certain voltage harmonics are completely eliminated.

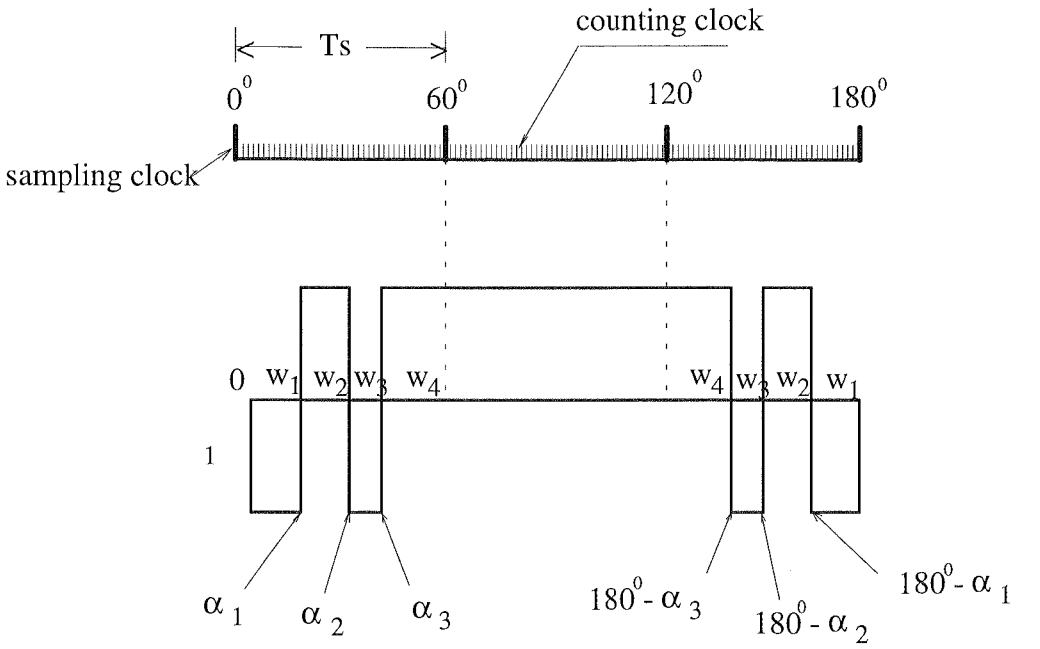


Fig 4.6, Principle of the harmonic eliminate technique

As a preliminary step for the optimisation procedure, the voltage in fig 4.6 is represented by it Furrier series :

$$f(\omega t) = \sum_{n=1}^{\infty} [a_n \sin n\omega t + b_n \cos n\omega t] \tag{4.11}$$

where

$$a_n = \frac{1}{\pi} \int_0^{2\pi} f(\omega t) \sin n\omega t d\omega t \tag{4.12}$$

$$b_n = \frac{1}{\pi} \int_0^{2\pi} f(\omega t) \cos n\omega t d\omega t \tag{4.13}$$

For quarter-cycle cosine symmetry,

$$a_n = \frac{1}{n\pi} \left[1 + 2 \sum_{k=1}^{M} (-1)^k \cos n\alpha_k \right] \tag{4.14}$$

$$b_n = 0 \tag{4.15}$$

If voltage control and elimination of fifth and seventh harmonics are desired, then :

$$a_1 = \frac{4}{\pi} [1 - 2\cos\alpha_1 + 2\cos\alpha_2 - 2\cos\alpha_3] \tag{4.16}$$

$$a_5 = \frac{4}{5\pi}\left[1 - 2\cos 5\alpha_1 + 2\cos 5\alpha_2 - 2\cos 5\alpha_3\right] = 0 \qquad (4.17)$$

$$a_7 = \frac{4}{\pi}\left[1 - 2\cos 7\alpha_1 + 2\cos 7\alpha_2 - 2\cos 7\alpha_3\right] = 0 \qquad (4.18)$$

Equation(4.16) and (4.18) are solved to generate the look-up table and stored in memories. Again, because of the symmetry and absence of notch in the middle of the wave, only the pattern for the 0 - 60 segment need be stored , and three phase full wave PWM outputs can be generated by appropriately locating address pointer.
Studies in [17] shows that the maximum magnitude of the fundamental is only about 93 percent for complete elimination of the fifth and seventh harmonics. As a result of elimination of lower order harmonics, the higher order significant harmonics such as eleventh and thirteenth become prominent. An improvement performance can be obtained by solving harmonic heating loss for different harmonics as a function of the notch angles and then iterating the angles so that loss (ie. the rms ripple current) is minimum. The effects resistance, though, varies as a function of temperature, and skin effect is assume to be constant.
The harmonic eliminate operation typically extend from 80 percent of the fundamental voltage, and the wave pattern characterised by the α angles are stored in 1 percent increment which may be adequate for system requirements. The lower step size is limited by the resolution of α angle implementation. At about 93 percent of fundamental voltage, $\alpha 1$ approaches to zero, and from this point, the voltage is increased by a one percent step by symmetrically shifting the notch toward the edge of half cycle and simultaneously reducing their widths

4-2-2, PWM operation modes.
According to discussions in obvious sections, the modes of PWM-IM operation will now be described with the help of fig 4.10 :
* a < a1 : f1 is lower than rated frequency of IM. PWM operates in the asynchronous mode. The carrier frequency fc is maintained as highest as possible to reduce effects of harmonics.
* a = a1 : frequency modulation index p reaches limited value. Therefore, fc must be reduced to fc1. However, fc1 must be sufficiently large to maintain a nearly sinusoidal motor current.
* a1 < a < a2 : the system shifts to synchronous mode, ie fc is changed synchronously with f1 at a constant ratio p1.
* a = a2 : the fc become large enough to violate the minimum notch time restriction. Therefore, fc must be reduced.
* a2 < a < a3 : system also operates in synchronous mode but ratio between fc and f1 is changed to p2.
* a = a3 : the operation is brought close to the boundary of the sinusoidal PWM, ie $m \approx 1$. From this, the system is shifted to harmonic elimination mode
The project employs a single microcontroller M68HC11 with speed of 2 kHz. Therefore, the maximum carrier frequency fc is also limited by capability for control calculation time of M68HC11. Estimated processing time for both feedback control function and PWM modulator is 1000μs (see also chapter 6 - System software implementation). Here, the maximum fc is limited within 1000 Hz, or 1KHz. As

shown in fig 4.6, the maximum fc is chosen 960 Hz at synchronous mode and 1 kHz at asynchronous mode.

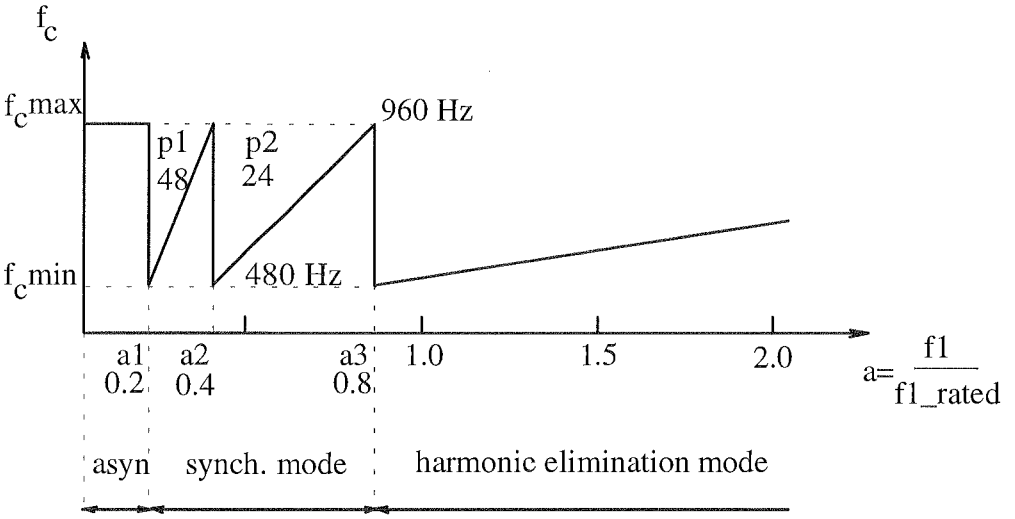


Fig 4.7, Modes of PWM-IM operation

Frequency index p is chosen equal to multiple integer of six (section 4-1-1, eq (4.5)). The best choice of p at synchronous are 24 and 48 as in fig 4.6. The maximum carrier frequency fc therefore is 480 Hz.

In summary, this chapter discusses aspects of the design of high performance PWM modulator using microcontroller in the wide range of variable frequency. The six step technique is also overviewed and it shows that although six step technique is a well-established technique, there has been important disadvantages that go some way towards reducing the performance of output waveform. The PWM technique is produced to overcome theses problems. Along with advances in the development and production of the microcontroller and power device, the PWM strategy has been continuously evolved and improved.
This chapter shows that the PWM technique can be grouped into two categories : uniform sampling and harmonic selection. In the former group, the main interest is that it is easy to implement in the form of digital circuitry and normally applied at low frequency. In the latter group, some relating functions are applied to eliminate subharmonics at output waveform. This group can be used from medium to high frequency.
The time constrain of power device and microcontroller is the main limitation of the PWM technique. The maximum carrier frequency is limited depending on the switching time of power device and speed of microcontroller. The best policy for carrier frequency is a sophisticated matter involving both power device and microcontroller and therefore also discussed in this chapter.

Chapter 5 : System hardware design

A fully digitalised PWM-IM transvector control system using microcontroller and standardised hardware circuits is described in this chapter. The first section overviews of system operation. The next section discusses hardware system implementation and the last section analysis speed and current sensors.

5-1, System operation :

The configuration of the proposed PWM-IM system was shown in section 2-2, fig 2.10 and 2.11 and now is redraw as in fig 5.1 in which the transvector technique is used to perform closed loop control system and PWM technique is employed to perform PWM voltages.

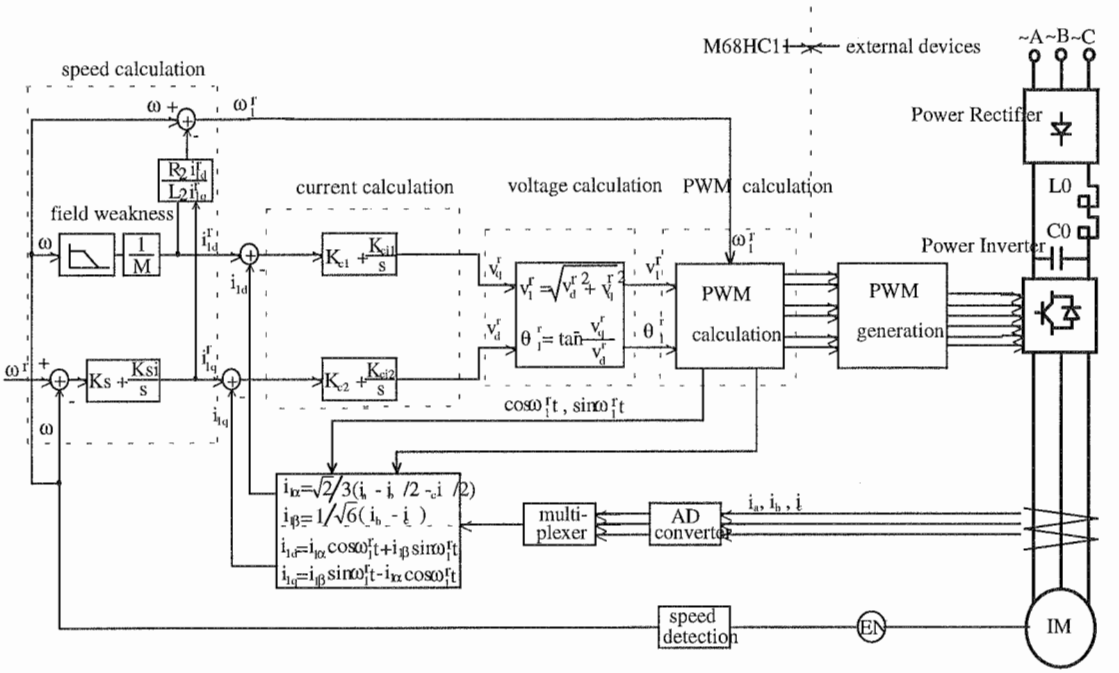


Fig 5.1, Block diagram of PWM-IM transvector control system.

5-1-1, Closed loop control system operation:

As shown in fig 5.1, closed loop control system is composed of a current detection, a speed detection, a speed controller two current controllers and some function calculations to ensure the transvector technique.

+ Detection processing:

In the detection processing, the motor speed is calculated by counting encoder pulse and the motor currents are decomposed by using current detection devices as shown. Encoder pulses are generated directly while motor currents are generated via AD converter and multiplexer.

It is difficult to process the ripple contained in the motor currents; hence, a improved current detection method is required for motor current detection.

Ref [18] developed an improved current detection method which included attention to current ripple components due to switching operation of the PWM inverter. Its principle is shown in fig 5.2.

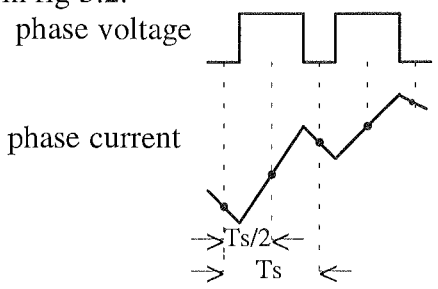


fig 5.2, Principle of current detection.

As expressed in fig 5.2, the switching of the PWM inverter occurs only twice in a sampling period Ts. In the proposed method, the current detection timing is synchronised with the point at the beginning and in the middle of the sampling period Ts. In this way, the current value at midpoint can be detected. As a result, the effective current value is obtained with very little ripple components.

+ Speed processing :

Speed controller accepts speed reference ω^r every time speed detection is performed and executes the speed control processing to obtain a torque current reference i_{1q}^r . A digitalised PI controller (its parameters are determined in chapter 3) is used for speed control. The amplitude of the magnitude flux, corresponding with motor speed, is determined at the same time. This value is assumed to be the magnetising current reference i_{1d}^r . Then, the slip angular frequency reference is calculated by eq (2-20) to ensure the transvector control law :

$$\omega_{sl}^r = \frac{R_2 i_{1q}^r}{L_2 i_{1d}^r} \tag{5.1}$$

This frequency reference and the detected motor speed ω are added to obtained the PWM inverter angular frequency reference ω_1^r :

$$\omega_1^r = \omega_{sl}^r + \omega \tag{5.2}$$

Finally, these process results are written into the common memory.

Speed processing is repeated every time speed detection is perform, ie at every sampling period of system.

+ Current and voltage processing:

Current control blocks read out the reference value of the torque current i_{1q}^r and magnetising current i_{1d}^r from the common memory to execute current control algorithms. As a result of the two current component control, V_{1q}^r and V_{1d}^r are obtained, then V_{1q}^r and V_{1d}^r are converted to a voltage amplitude reference V_1^r and phase reference θ_1^r by the vector calculation :

$$V_1^r = \sqrt{V_{1d}^{r\,2} + V_{1q}^{r\,2}} \tag{5.3}$$

$$\theta_1^r = \tan^{-1}\frac{V_{1q}^r}{V_{1d}^r} \tag{5.4}$$

ω_1^r, V_1^r, and θ_1^r are reference values of the voltage frequency, amplitude and phase which are fed to PWM calculation and PWM generation.
Current and voltage processing are repeated at every time current component detection is performed , ie they are executed two time faster than speed processing.

5-1-2, PWM modulator operation.
The project employs uniform sampling technique for system from stand still up to rated motor speed and harmonic selective technique for system at higher 0.8 motor rated speed. Modes of PWM operation is analysed in detail in chapter 4 and shown in fig 4.6.
In the context of this section, the function of the PWM modulator is divided into two parts. One is to determine the delay time td , pulse width time tw of each pair of the power semiconductor element. Another is to generate the gate pulse at some determined time. The former function is calculated by microcontroller while the latter is performed mainly by hardware counter.
The basic hardware configuration of the PWM modulator is shown in fig 5.3.

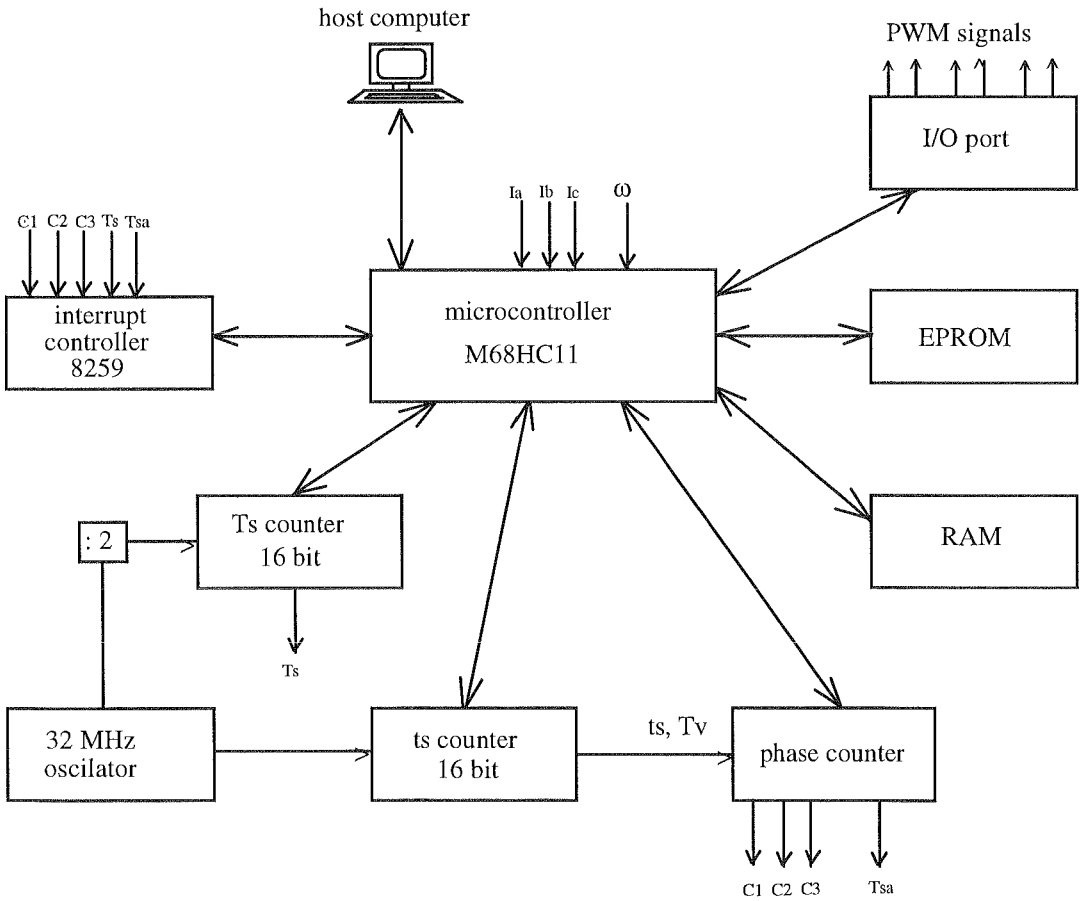


Fig 5.3, Simplified hardware of PWM modulator.

In fig 5.3, 8Kbyte EPROM is used to store the look-up table of the pu sine data base. A 8 bit programmable phase counter is used as the pulse width counter and 16 bit counter Ts generates the interrupt signals for a interrupt controller at every sampling period. All the PWM output signals with phase polarity are interfered through the synchronising flip-flop to prevent any timing error.
In the operation, the microcontroller reads the reference value ω_1^r, V_1^r, and θ_1^r from memory, and clock frequency data which is proportional to ω_1^r is set to counter Ts and ts. The counter Tp counts clock pulse ts and determines the flux vector phase value $\omega_1^r t$ at time t. Then, the phase of the modulator signal is calculated by adding a phase reference value θ_1^r to $\omega_1^r t$.
The instantaneous amplitude of the modulator is determined by using look-up table and an amplitude reference V_1^r as following formula :

$$v_1^r = V_1^r \sin(\omega_1^r t + \theta_1^r) \qquad (5.4)$$

Then, the delay time td and pulse width time tw are calculated by eq (4.6) through (4.10). After that, the microcontroller sets the data which correspond to td and tw in the 8 bit programmable phase counter. This processing is executed for three phases. Phase counter is prepared for each phase. Finally, PWM signal are sent to synchronising circuitry and $\sin\omega_1^r t, \cos\omega_1^r t$ are written into RAM memory to use for current detection which is executed next.
As explained, the PWM modulator combines software processing and the hardware counter . Therefore, it has two features : generation of an arbitrary PWM signal is possible by modifying the software program; and resolution obtained for the PWM signal generation is higher.

5-2, Control system hardware design.

A simplified hardware block diagram of PWM-IM vector control system is shown in fig 5.4. The microcomputer is based on the M68HC11 and a single board with appropriate peripheral hardware built up to do functions of modulator and feed back control.
The C language program, including look-up table, is contained in 8K of EPROM memory, and it is supported by 8K of RAM. The chip are used as three phase pulse width and Tsa counter which generate the interrupt signal for 8259 chip. All the PWM output signals with phase polarity are interfaced through the synchronising flip-flop to prevent any timing error. The high speed Ts and ts timing counter use Schottky TTL chip and are triggered by a 32 MHz oscillator as shown.
To get a better idea of control hardware design, some symbols are used and should be explained before looking at in detail. As shown in fig 5.4, each box contains a small number in their low-right corner. This number tells that the detail schematic for these parts will be found on sheet with that number (appendix C). The next point to look at are the number in each box. In addition to apart number such as 138, each box has a number of the form A3. This second number is used to help locate the IC on the printed circuit board.

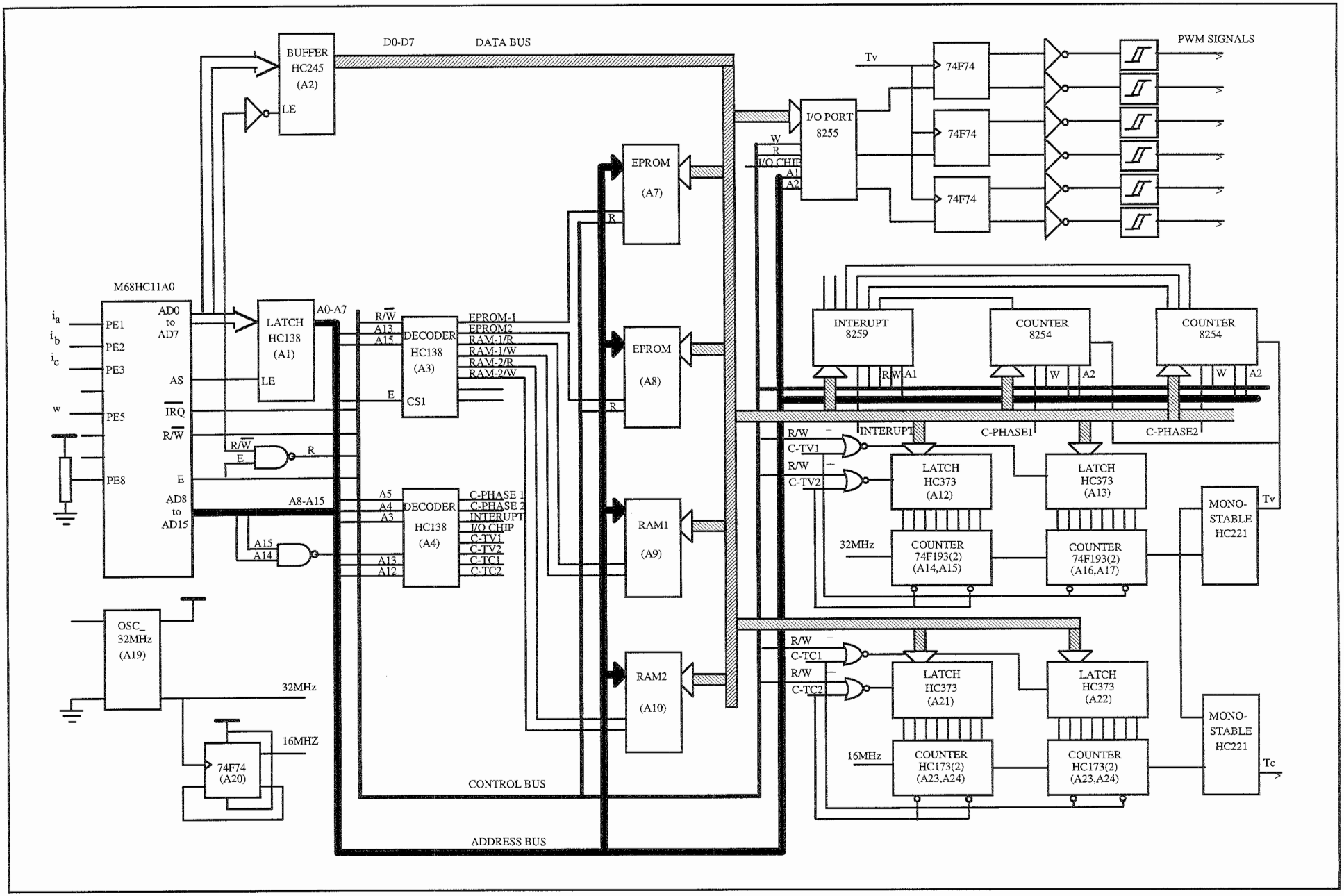


Fig 5.4, Detail block diagram of PWM modulator

5-2-1, Overview of control system hardware.

The first part to look at in fig 5.4 is the M68HC11 microcontroller. The M68HC11 microcontroller accepts and processes speed and current feed back signals and motor speed reference from host computer or ROC. Then it produces address bits and data bits depending the function it is executing.

The next parts to look for in the block diagram of the control system hardware are address latch (A1) and data buffer (A2). Address latch is needed to grab address information produced by microcontroller. A heavy black line is used to distinguish the demultiplexer address bus from data bus.

Following the address line to the of the address latch to find memory of the system (A7 to A10) and memory decoder A3. The memory decoder connected to EPROM/RAM memory has two related purposes. The first is to produce a signal which turns on the desired EPROM or RAM. The second purpose is to make sure that only once device is outputting on data bus at a time.

The box just below memory decode is port decoder A4 that has somewhat the same purpose with memory decoder. However, it is used for decoding external device such as phase counter, interrupt controller, etc.

A set of latches A12, A13 and 4 bit counters A14 to A17 performs 16 bit counter while another set from A18 to A 21 performs 16 bit Ts counter.

The output pulses of ts and Ts counter are put through monostable to expand their duration before sent to phase counter A12.

System output is expressed on the top of the diagram. It includes a programmable parallel port, and six flip-flop to synchronising output waveforms. Finally, six opto-isolation are used to isolate control system from power inverter to avoid any damage.

5-2-2, M68HC11A0 controller : (fig 5.5)

Power supply : connected to pin Vdd (+5V) and Vss (ground). The 1μF capacitor (C6) and 0.01 μF capacitor (C4) are used to provide good power supply bypassing at the MCU. Both these capacitor should be as close (physically and electrically) as possible to the M68HC11A0 and should have good high-frequency characteristics (ie, not old technology dipped ceramic disc). The separate 0.01 μF capacitor is included because the large 1μF capacitor is typically not as good at snubbing very high frequency noise.

The 1 μF capacitor (C5) primarily supplies charge for bus switching through a very low impedance path. Without this bypass, there could be very large voltage drops in the circuit-board runner to the MCU due to the very high current spike caused by several MCU pins simultaneously switching from one level to the other.

Mode select pin (MODB/VSTBY and MODA/LIB) : Because MCU is used in the expanded mode, the mode select pins MODB an MODA must be high. To do this, 4.7K resistor R11 and R12 are used. However, a connect Jumper J1 could be used to pull MODB down for test mode.

Crystal oscillator pins (EXTAL and XTAL): a crystal oscillator of 8 MHz is used. The resister R13/10M provides direct current bias to the inputs. Two equal capacitor C1 and C2/18pF are combined with the higher output impedance in order to limit the power into the crystal.

Clock pin (E) : is the bus frequency clock output and four time lower than crystal frequency (equal to 2 MHz in this case). This pin can be used to control external

devices. When E is high, data is being addressed. When E is low, an internal process is occurring.

Reset pin (RESET) : connected to manual button via low voltage inhibit (LVI) MC34164 to reset M68HC11 system. M68HC11 is initialised when reset pin is low.

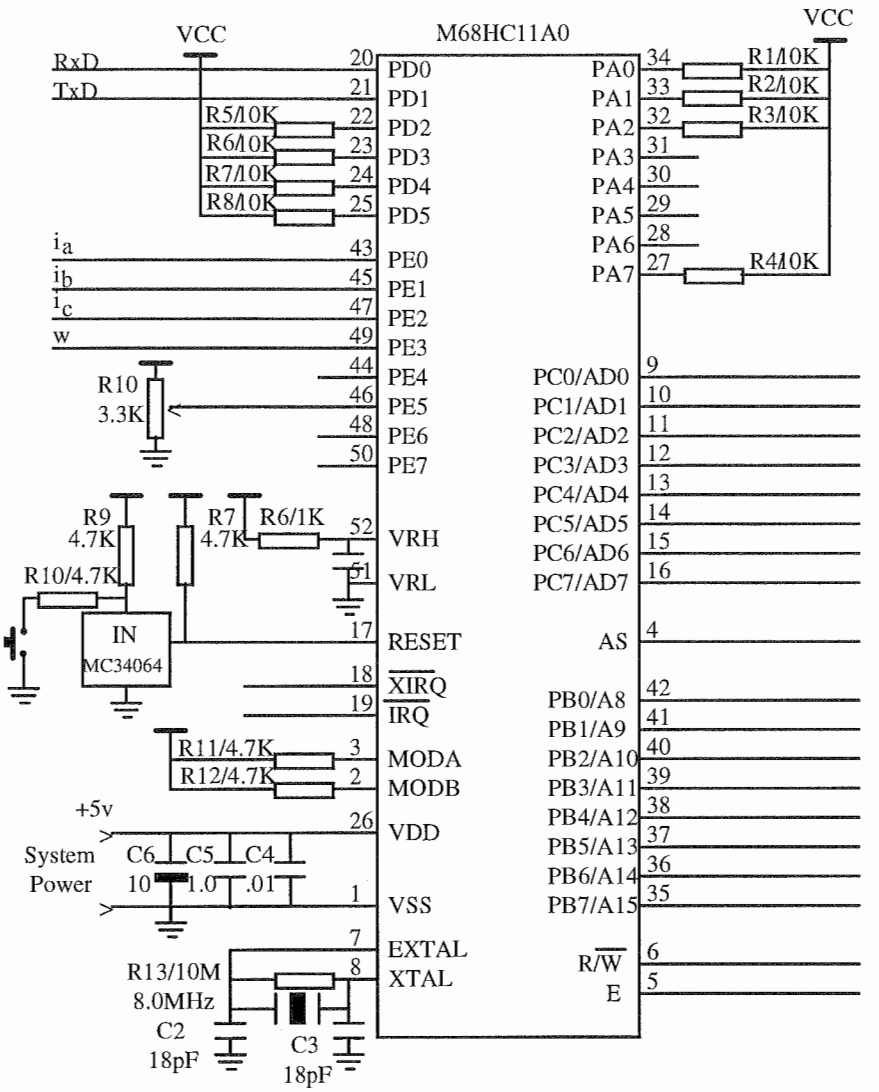


Fig 5.5, M68HC11A0 connection.

Interrupt pins (XIRQ,IRQ) : XIRQ pin when active low, provide a means for requesting nonmaskable interrupt whereas IRQ pin, active low, provides a means for requesting asynchronous interrupts.

A/D reference pins (VRH,VRL) : these pins provide the reference voltage for the a/d converter circuitry. To ensure full A/D accurate. The voltage between VRL and VRH must be at least 2.5V.

A low pass filter R6/1K and C1/1u is to isolate noise on the logic power supply from the relatively sensitive analog measurement.

A/D input port (port E) :

+ Port PE0,PE1 and PE2 are used to read three phase current ia,ib and ic.
+ Port PE3 read motor speed ω.
+ Port PE5 read reference speed w via resistor R10/3.3K

Serial port (port D) : provides a means for serial communication with host computer.
Multiplexer address/data bus (port C) (see fig 5.8, timing operation). Timing during first haft of bus cycle E, address output signal A7-A0 are presented on these pins (port C). During second haft of E, these eight pins are used as bidirectional data bus.
Address enable pin (AS) : is used as active high latch enable to an external address latch (see also fig 5.8) for expended mode timing). From fig 5.8, it can be seen that when AS is high, address information is allowed through external address latch and it is latched when AS is low.
Termination unused pins : some input on the MCU can be float (unconnected) as shown. However, many other can not be left unconnected. They must be pull up through a resistor of 10K.

5-2-3, Address latch 74HC373 (Fig 5.6) : because port C is used as multiple address/data bus, an external latch 74HC373 is needed to grab address at first haft cycle E and hold them at the second haft cycle E. The AS signal is used to trobe latch at the proper time (see also fig 5.8). Once the address is stored on the output of latch, the MCU removes the address from port C and used this port for reading or writing data.

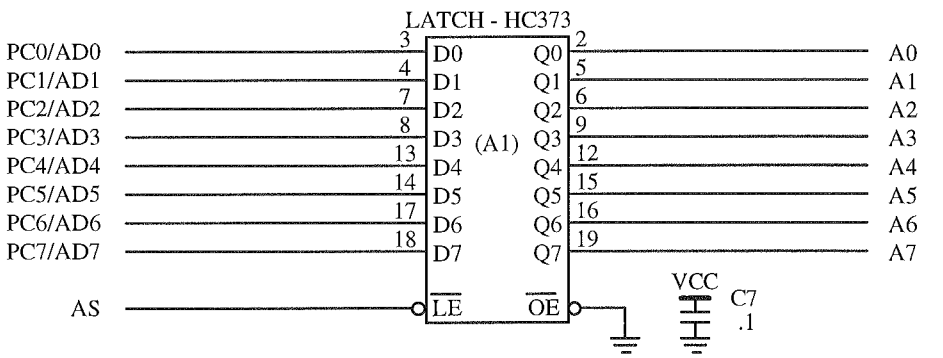


Fig 5.6, Address latch

5-2-4, Data buffer 74HC245 (Fig 5.7) : most of the external devices (ROM, RAM, ENCODER, etc) connected to MCU have MOS inputs. Therefor, on a dc basis, they do not require much current. However, each input or output added to system data bus acts like a capacitor of a few pico fara connected to ground. In order to charge the logic state these signal from low to high, all these added capacitances must be charged. To change the logic state to low, the capacitances must be discharged. If more than a few devices on the data bus lines, the MCU outputs can not support enough current drive to charge and discharge the circuit capacitances fast enough. Therefore, data buffer 74HC245 is added to do this job.
Because M68HC11 does not have data enable line DEN and data trans/receive line DTV, we use AS line and R/W line as shown. When AS goes low, it enables 74HC245 and R/W line will determine data direction :

Read : R/W = 1 ---> DIR = 0 ---> data from B to A
Write : R/W = 0 ---> DIR = 1 ---> data from A to B.

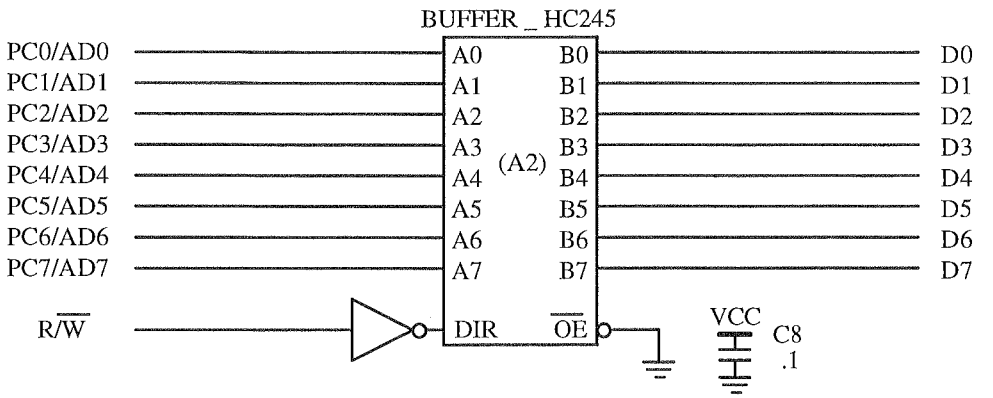


Fig 5.7, Data buffer

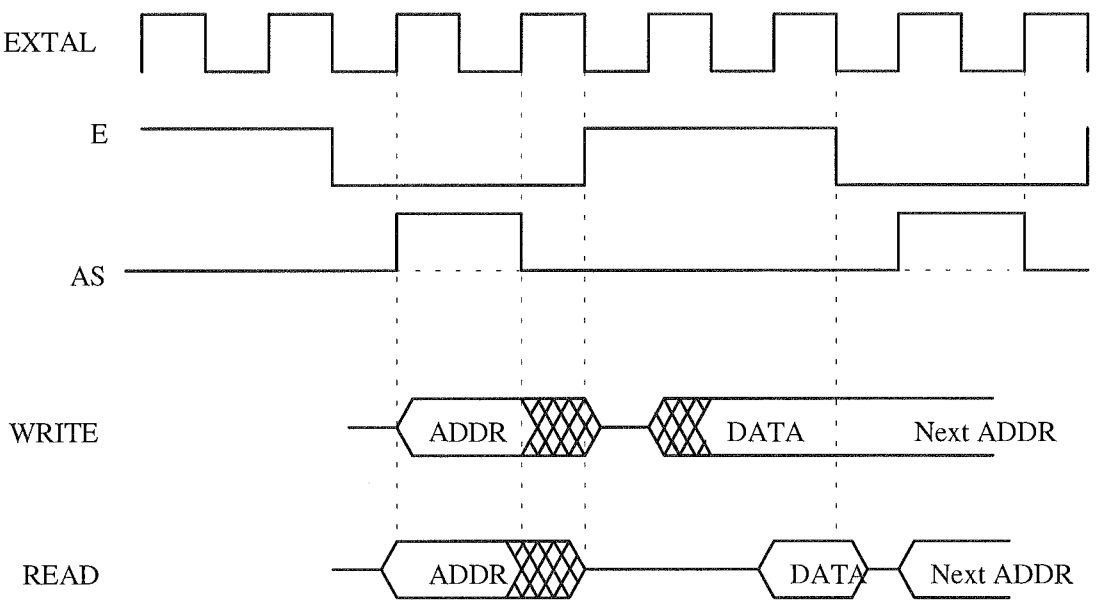


Fig 5.8, Expending mode timing- port C

5-2-5, Decoder 74HC138 : Some 74HC138 in the system serves as decoder. As mentioned while discussing the block diagram of system, there are two function related to decoder : one is to produce a signal which enable the device that is wanted to enable for a particular address. Another function of decoder is to make sure only one device at a time is enable to read or write data from data bus lines.

As shown in block diagram of system, fig 5.4, system includes two decoders :

+ Memory decoder.
+ Port decoder.

Address mapping and decoding : As shown in the fig 5.4, the system contain two EPROM 8K×8, two RAMs 8K×8 and eight external devices : two phase programmable counters C-PHASE1 and C-PHASE2, two components of 16 bit down counters C-TV1 and C-TV2, two another components of 16 bit down counter C-TS1 and C-TS2, parallel port 8255 I/O PORT and finally a programmable interrupt 8259 INTERRUPT. The address mapping for each of them is shown in table5-1 and Fig 5.9

Table 5.1 : Address mapping for external devices.

			Hex-digit				Hex-digit				Hex-digit				Hex-digit				Hex
			2^{15} A_{15}	2^{14} A_{14}	2^{13} A_{13}	2^{12} A_{12}	2^{11} A_{11}	2^{10} A_{10}	2^{9} A_{9}	2^{8} A_{8}	2^{7} A_{7}	2^{6} A_{6}	2^{5} A_{5}	2^{4} A_{4}	2^{3} A_{3}	2^{2} A_{2}	2^{1} A_{1}	2^{0} A_{0}	
Memory	EPROM-1	Start	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF
		End				0	0	0	0	0	0	0	0	0	0	0	0	0	E000
	EPROM-1	Start	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	DFFF
		End				0	0	0	0	0	0	0	0	0	0	0	0	0	C000
	RAM-1	Start	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	7FFF
		End				0	0	0	0	0	0	0	0	0	0	0	0	0	6000
	RAM-2	Start	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	5FFF
		End				0	0	0	0	0	0	0	0	0	0	0	0	0	4000
External devices	C-PHASE 1		0	0	1								0	0	0				2FFF
	C-PHASE 2												0	0	1				
	INTERRPUT												0	1	0				
	I/O PORT												0	1	1				
	C-TV1												1	0	0				
	C-TV2												1	0	0				
	C-TC1												1	1	0				
	C-TC2												1	1	1				2000

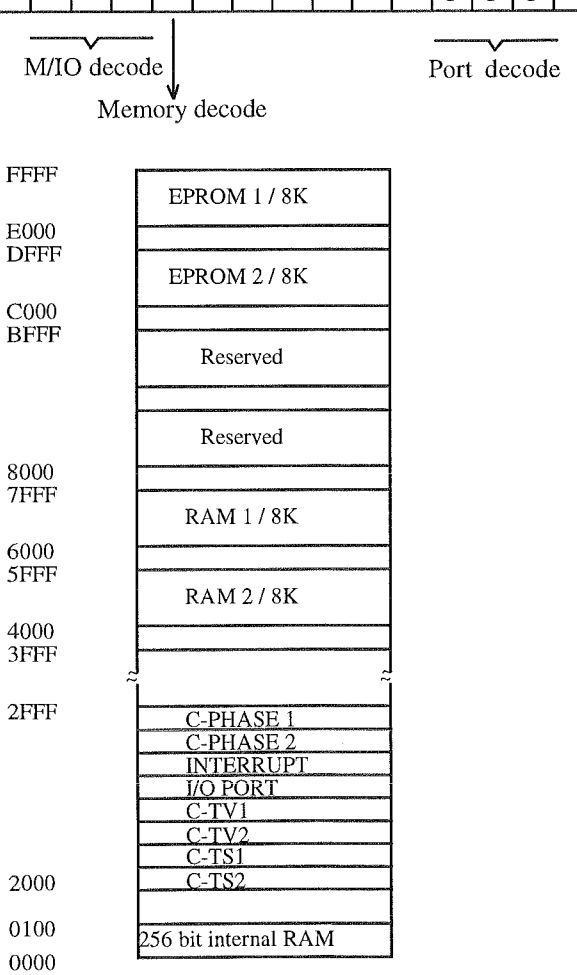


Fig 5.9, Address mapping and decoding

Memory decoder : is used to decode memory. One of the disadvantages of M68HC11 is that R/W pin is not compatible with Intel devices. In order to save pin, M68HC11 uses only one R/W pin to provide both READ and WRITE signal whereas Intel devices require two separate READ and WRITE signals. To overcome this problem, a memories decoder is used to provide separate READ and WRITE signal for each memory. Table 5.2 expresses truth table of memory decoder and fig 5.10 - memory decoder circuitry.

Table 5.2 , Truth table for A6 : 74HC138 - memory decoder

Inputs							Outputs						
cs1	cs2	cs3	A2	A1	A0	y0	y1	y2	y3	y4	y5	y6	y7
(E)	(G)	(G)	a15	a13	r/w	W-ra2	R-ra2	W-ra1	R-ra1		R-ep2		R-ep1
1	0	0	0	0	0	0							
1	0	0	0	0	1		0						
1	0	0	0	1	0			0					
1	0	0	0	1	1				0				
1	0	0	1	0	0					0			
1	0	0	1	0	1						0		
1	0	0	1	1	0							0	
1	0	0	1	1	1								0

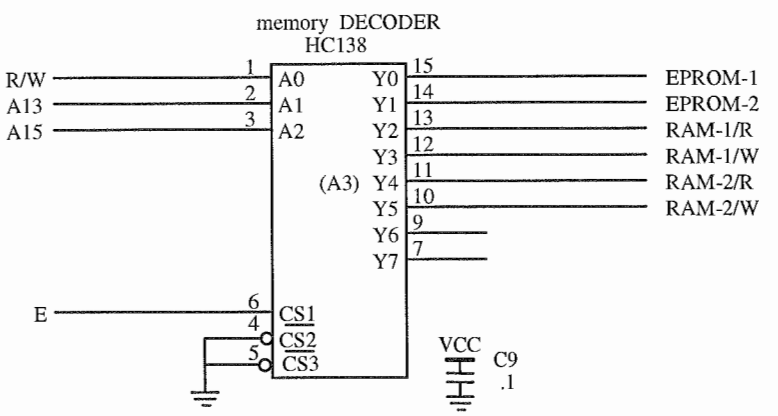


Fig 5.10 Memory decoder circuitry.

Port decoder : is used to select external devices other than memories. It uses codes A3, A4 and A5 to produce chip selects for 8 external devices. (see also address mapping table 5.1). Table 5.3 expresses truth table of port decoder and fig 5.11 - memory decoder circuitry.

5-2-6, EPROM : Two EPROM 8K×8 are used (fig 5.9). The EPROM 1 and EPROM 2 lines select chip and R-EPROM 1 and R- EPROM 2 provide read signals for EPROMs.

5-2-7, RAM :

Two RAM 8K×8 are used (fig 5.13). the RAM lines is to select RAM and R,W lines provide read and write signal for RAMs

Table 5.3 , Truth table for A3 : 74HC138 - port decoder													
Inputs							Outputs						
cs1	cs2	cs3	A2	A1	A0	y0	y1	y2	y3	y4	y5	y6	y7
(E)	(G)	(G)	a5	a4	a3	c-1	c-2	int	i/o	ts1	ts2	Ts1	Ts2
1	0	0	0	0	0	0							
1	0	0	0	0	1		0						
1	0	0	0	1	0			0					
1	0	0	0	1	1				0				
1	0	0	1	0	0					0			
1	0	0	1	0	1						0		
1	0	0	1	1	0							0	
1	0	0	1	1	1								0

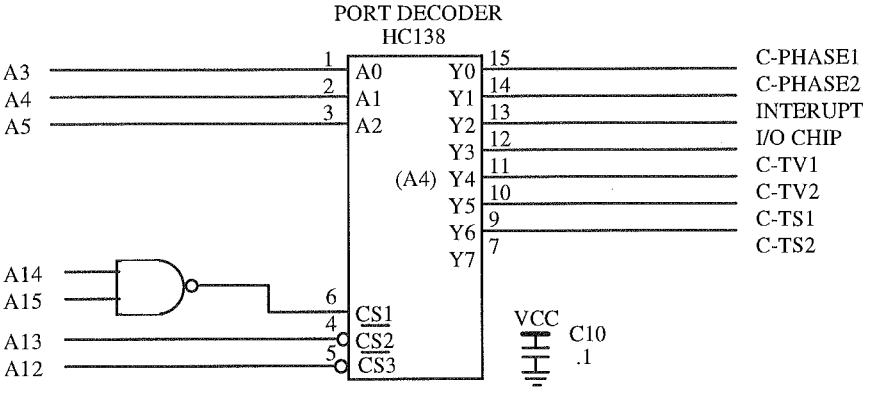


Fig 5.11, Port decoder circuitry.

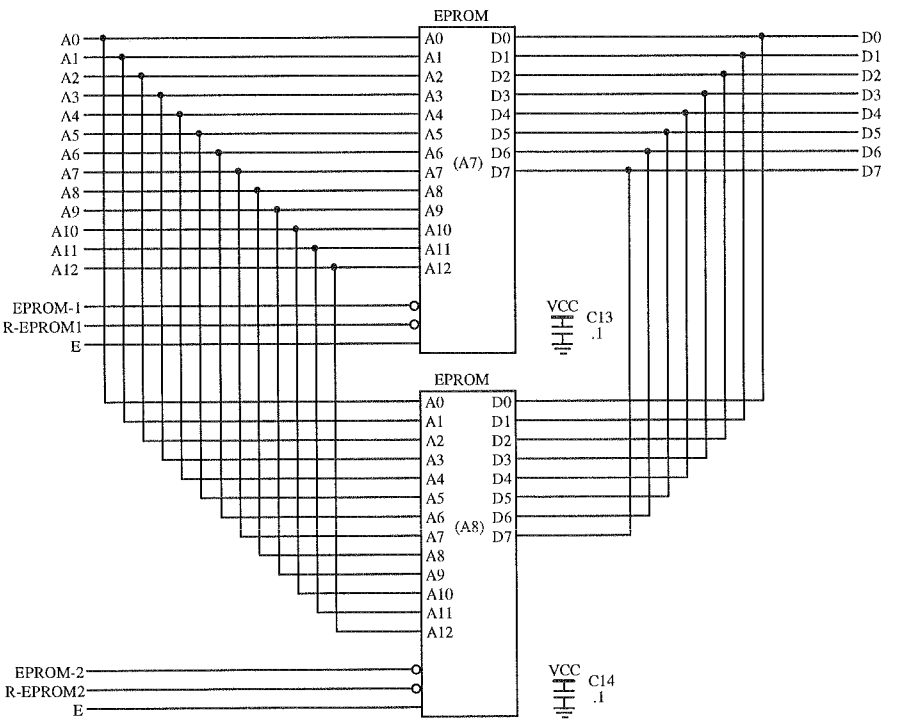


Fig 5.12, EPROM circuitry.

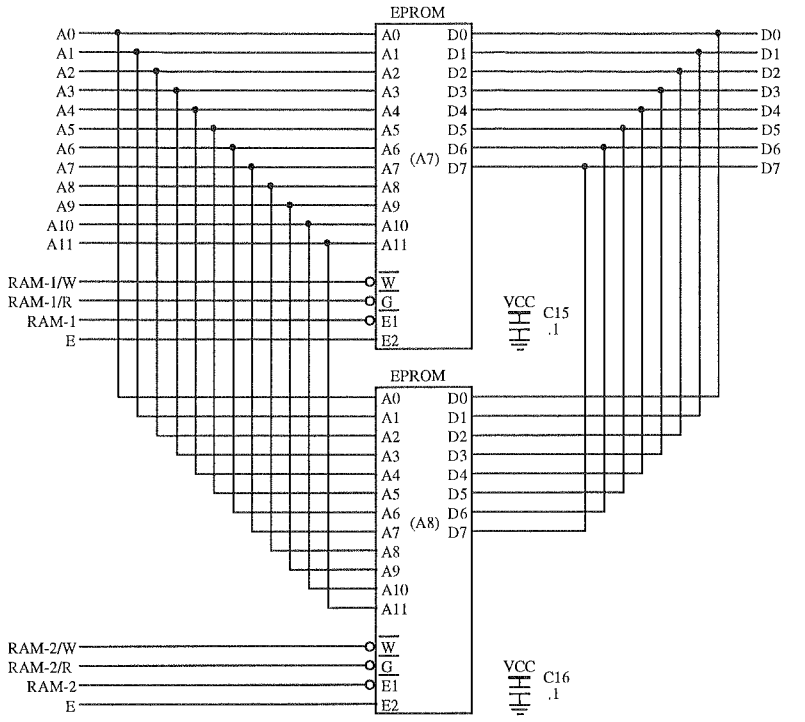


Fig 5.13 RAM circuitry

5-2-8, High speed oscillator :(fig 5.14).
An oscillator module with output frequency of 32 MHz clocked the counting clock that provides Tv. In addition, the frequency 32 MHz is scaled by two via a D-type flip flop 74F74 to provide frequency 16 MHz for Ts counter.

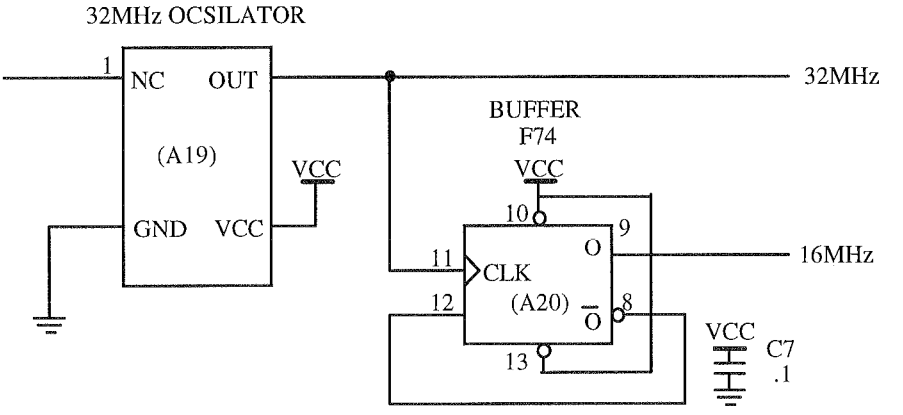


Fig 5.14, Oscillator

5-2-9, 16 bit down counter Tv and Ts : (fig 5.15 and 5.16)
Four cascaded 4 bit down counters were accepted for 16 bit programmable counter. Because Tv counter run at 32 MHz, 4 bit counter 74F193 is chosen. Another set of 4 bit counter 74HC193 is chosen for Ts counter because Ts counter is driven at lower frequency (16 MHz).
To hold counter word for each 16 bit down counter, two lathes 74HC373 are employed. The latches are controlled by R/W line and the appropriate enable input from peripheral address decoder.

Two NOR gates and two NOT gate are introduced to obtain appropriate control signal for latches and counters. The NOT gate also provide time delay so that counters can preset valid data from latches. The timing diagram for counter holding data from latches is estimated as in fig 5.17.

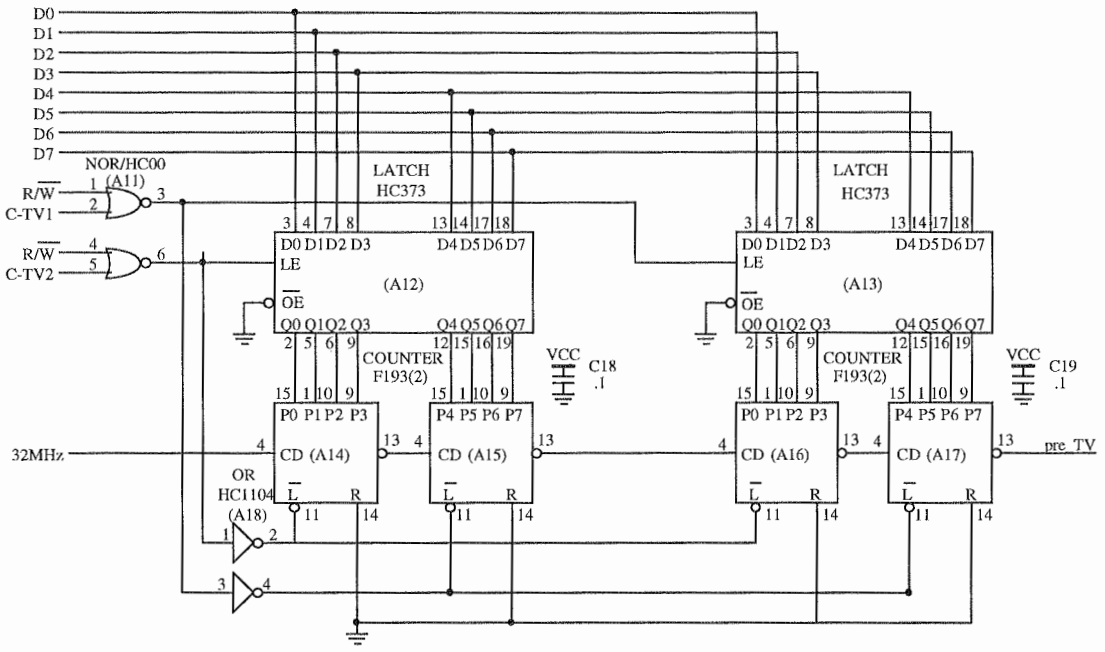


Fig 5.15, Tv counter

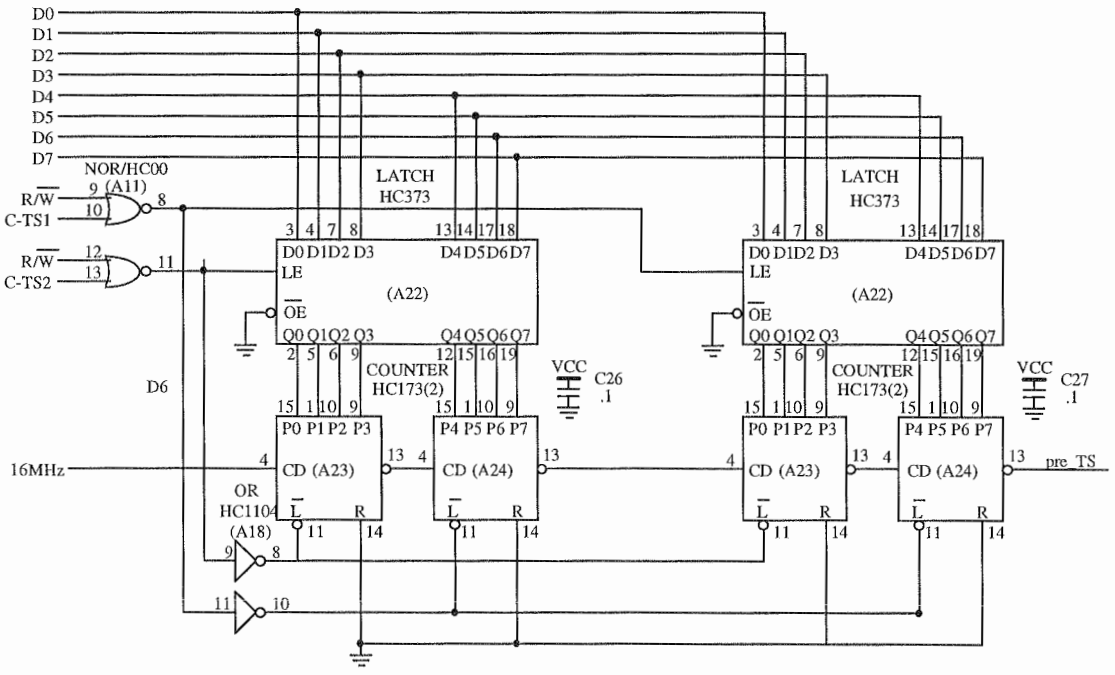


Fig 5.16, Ts counter

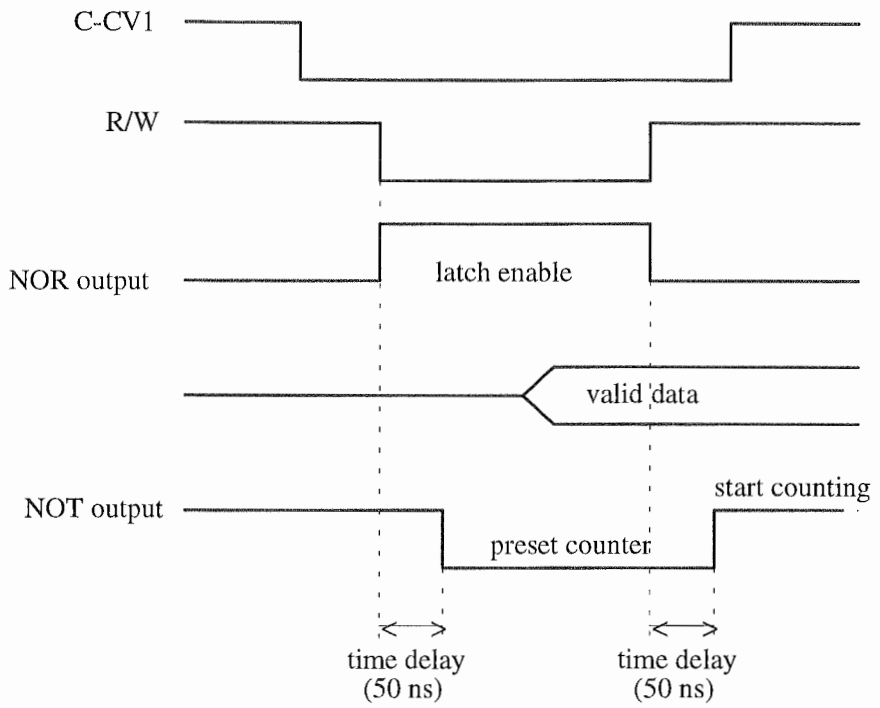


Fig 5.17, timing diagram for 16 bit down counter.

5-2-10, Monostable :

The terminating outputs of the most significant counters of each array are needed to be fed into a monostable 74HC221 to extend the duration of the pulse. The output pulses from sampling counters have to be a high going pulse, with pulse width being a minimum of 60 nanosecond in duration as this outputs drive an interrupt line. The terminating outputs from the counting clock has to be a high pulse of minimum pulse duration of 200 nanosecond as this clock driven four counters. Both pulse width are made equivalent to 250 nanosecond.

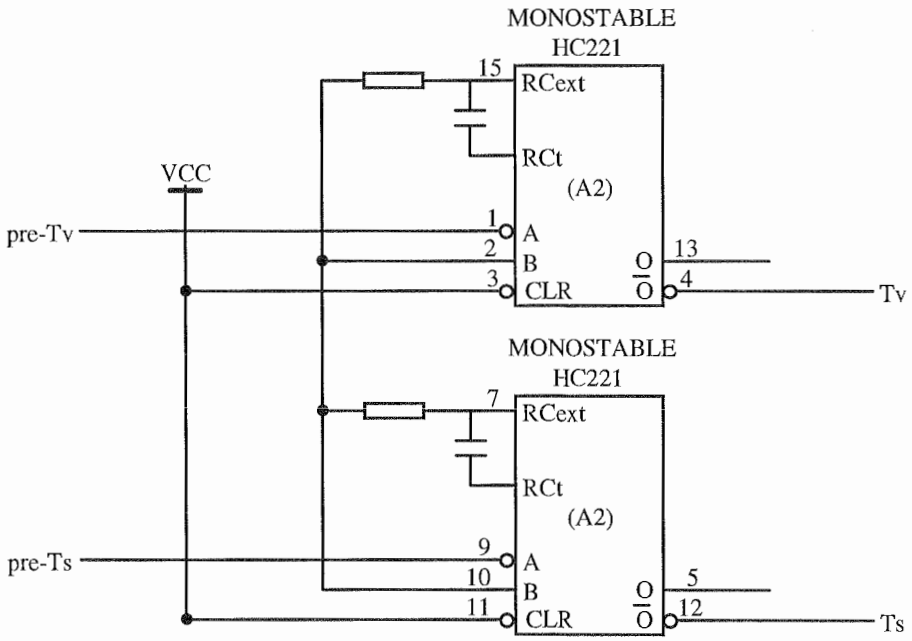


Fig 5.18, Monostable circuitry.

5-2-11, Programmable 8 bit counters:

Four programmable 8 bit counter are required : three are required to generate the pulse widths and delay times for three phase outputs, one is to trace the carrier period during asynchronous mode.

Two INTEL 82C53 Programmable counter are employed to satisfy these system requirements. Each chip contains three independently operating 16 bit counters which can be programmed to operate as 8 bit counters.

Three pulse widths counters are situates on a single 82C53 while Tsa counter occupy the other chip as shown in fig 5.19.

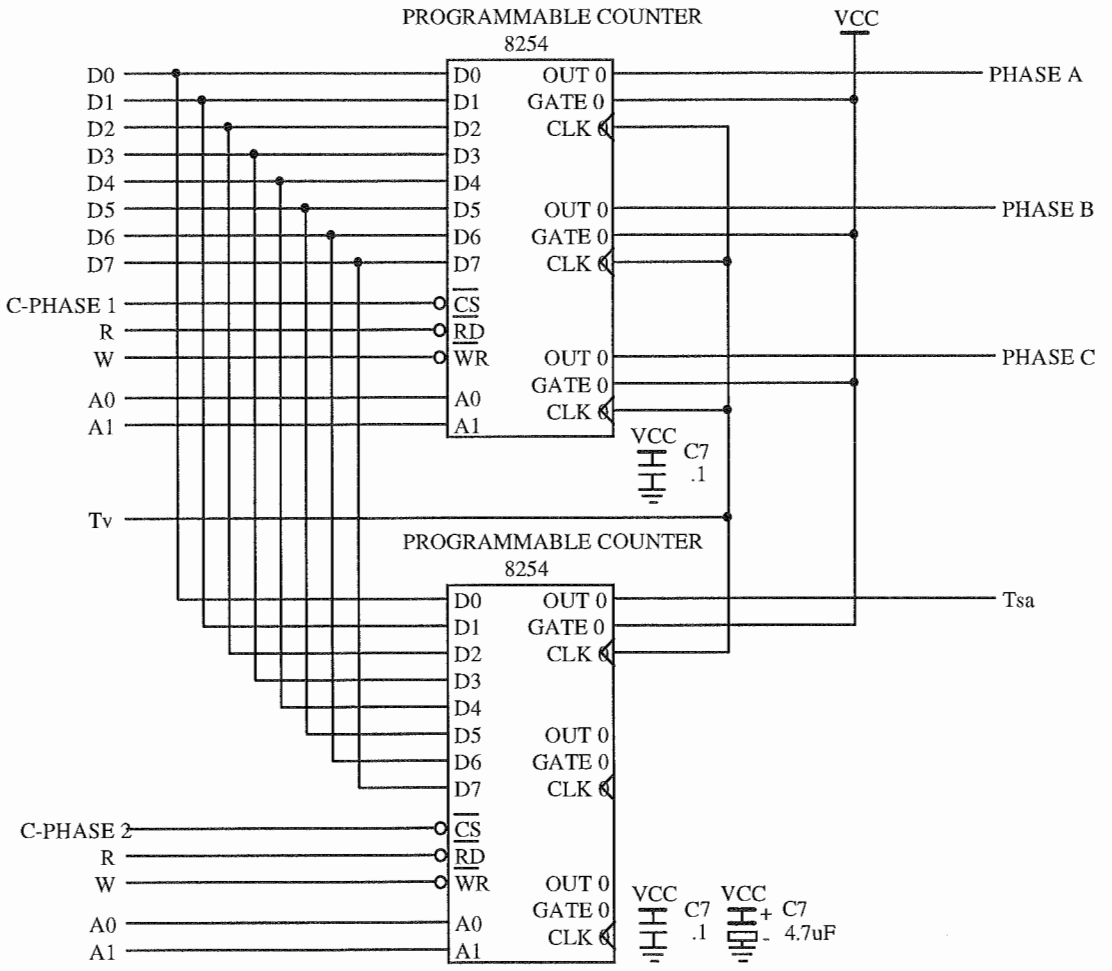


Fig 5.19 , Configuration of the 8 bit counter

All phase counter have been incorporated in the design assuming they are to operate as time-out counters, that is the OUT pin of each counter goes high on the termination of the counter are remains high until a new count is loaded. This is referred to as MODE0 operation. All counters on the other programmable counter must operate in MODE 2 where the OUT pin outputs a square wave with frequency equal to the driving clock divided by the count issued to the counter.

These modes of operation must be initialised by writing to the control register of each counter.

The OUT pins of the three phase counters and the Tsa counter drive are used to issue interrupt requests to the CPU.

5-2-12, Interrupt :

A maximum of five counters are required to issue interrupts to the CPU, which occurs during three phase, asynchronous, uniform sampling operation. These include the sampling clock Ts, the carrier clock Tv and three phase counters.

The programmable interrupt controller 8259 can provide up to eight interrupt inputs with programmable priority management and is directly interfaceable with the CPU. As only five input are required, the remaining three inputs are masked by software.

The programmer can specify the five most significant bit of this pointer. During initialisation, the controller inserts the three least significant bits automatically depending on the input request interrupt. Therefore, four address location must contain the new instruction pointer and code segment register relating to the start of the service routine.

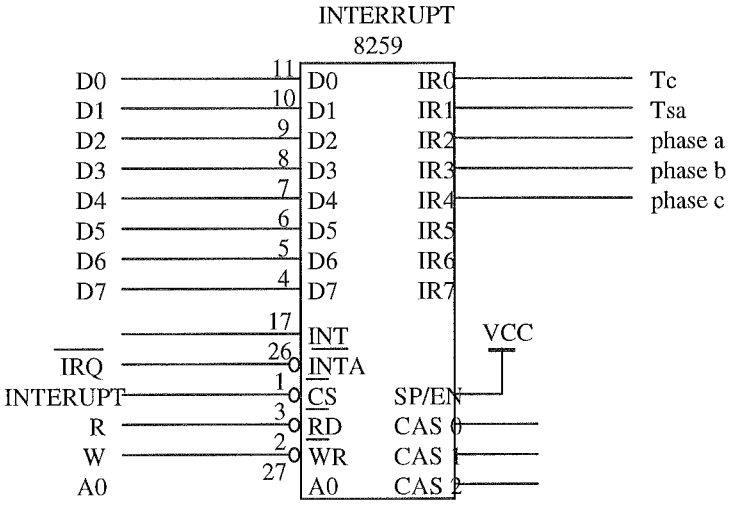


Fig 5.20, Interrupt

5-2-13, Interfacing circuitry :

The modulator is required to send logic signal to the power inverter via an isolation and driver circuit in order to turn the switching on/off to produce the correct PWM output.

+ Parallel interfacing port : the modulator utilise a programmable parallel interface (PPI) 8255 to provide interface. The PPI has three independently addressed 8 bit ports which can be configured to be output or input ports by software. The 8255 is to be configured as an all output port which can achieve by sending a control byte to the control register. Only three output to the PPI are required because the other signals, there exists six switching elements on the inverter, are simply complement of complement sign. This is because the series pairs of MOSFET's can not turned on simultaneously as a short circuit will occur causing damage to the MOSFET's.

+ Synchronising circuit : To prevent any time error, The output of parallel port are put through three D-type synchronising flip flop 74F74. The three flip-flop are clocked by the counting clock ts.

+ Isolation : provide protection to the digital circuit of the modulator if any power MOSFET becomes damaged.

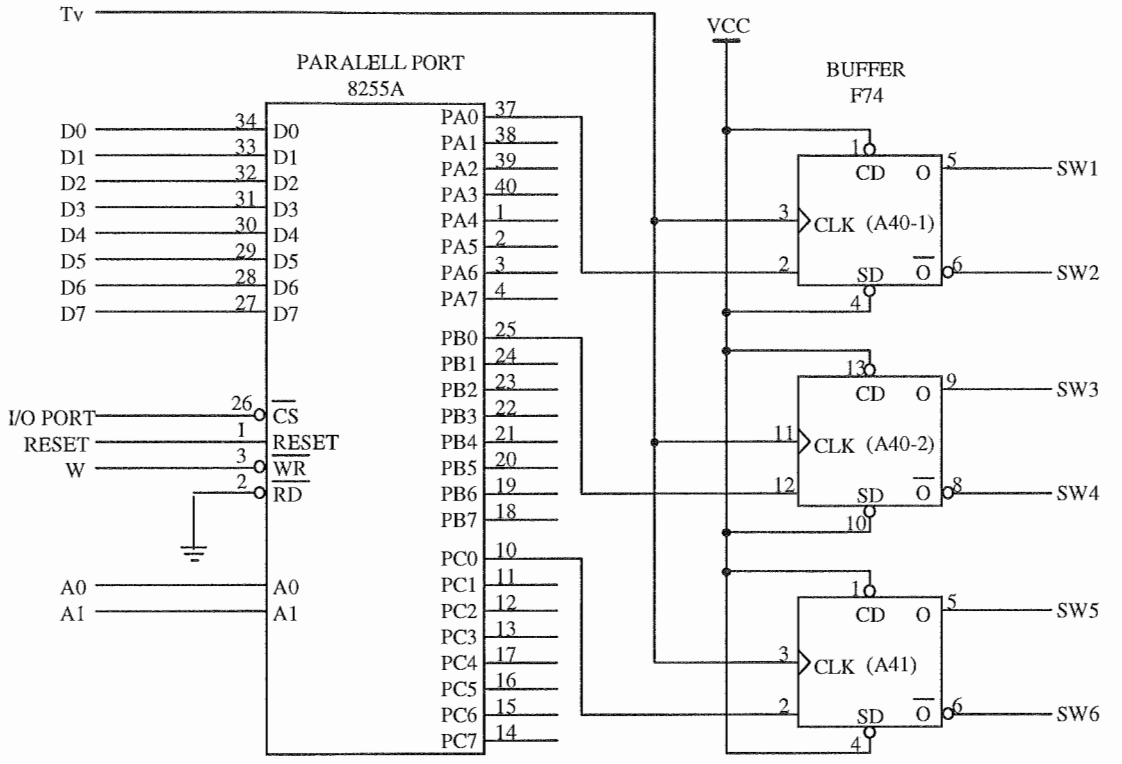


Fig 5.21, Output port.

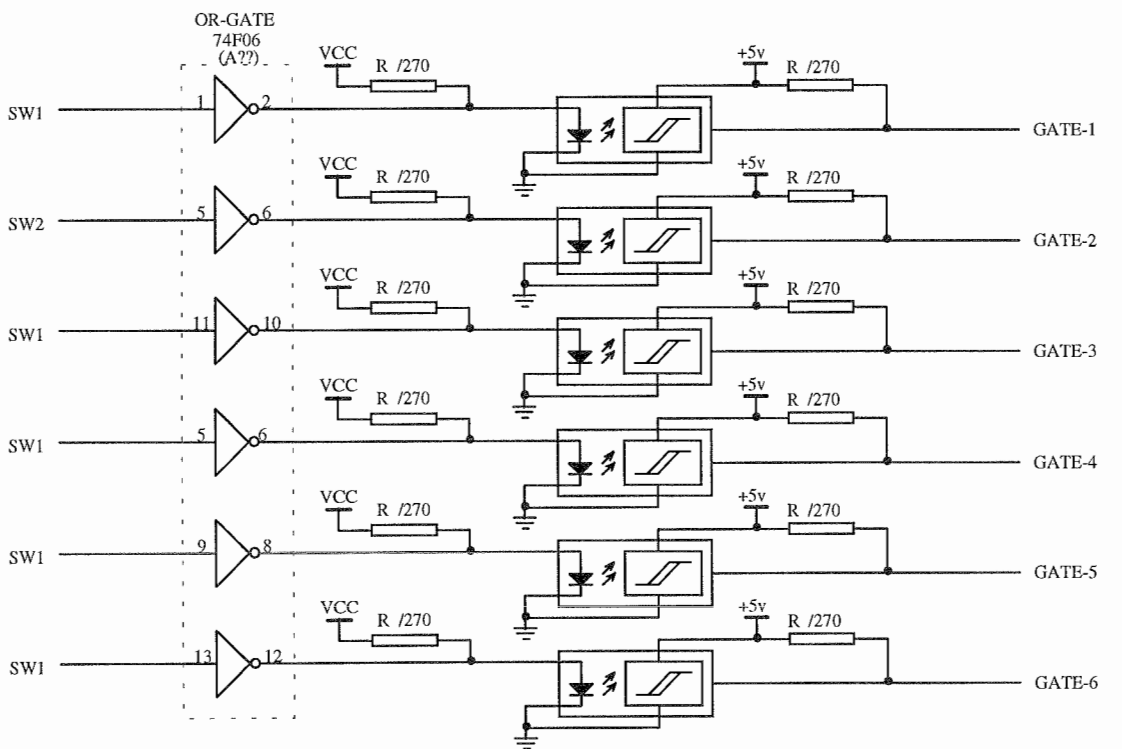


Fig 5.22 Isolation circuit.

5-3, Current and speed sensor.

5-3-1, Current sensor.

The project employs a three phase current detection available in the power lab. However, some aspects related to current detection should be included.
Normally, the motor current is detected by Hall effect current transducer. A device supplied by Honeywell Microswitch can be selected. This kind of device has three pins which can be connected as in [19]. The output from transducer is a voltage which is from 25% to 75% of the voltage supply and can be calculated by the following formula:

$$V_{output} = V_{offset} \pm \frac{(0.0364 \times N \times I)}{I_g} \times \frac{V_{cc}}{12} \times K \qquad (5.8)$$

Where :

V_{offset}	= output voltage at zero current.
N	= No. of the current carrying conductor passing.
I	= magnitude of current in the current carrying conductor.
Ig	= gap cut in the flux collector.
Vcc	= voltage supply.
K	= constant depending on Vcc.

The maximum motor current is 15 A. From eq (5.8), in order to obtain output voltage range 5V to 6V dc, 4 turn around the flux collector are required.

5-3-2, Speed sensor.

Shaft encoder is used in this project to detect motor speed. Fig 5.23 shows simplified configuration of motor shaft encoder.

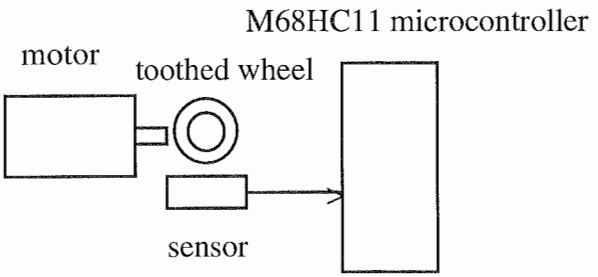


Fig 5.23, Simplified configuration of motor shaft encoder.

The principle of motor shaft encoder can be explained as follow : a toothed wheel is mounted on the motor shaft and an opto-switch generates pulse as motor shaft rotates. On the rising edge of each pulse, the microcontroller reads its free-running internal 16 bit counter- the input clock to this counter is driven from the primary microcontroller clock at 2 MHz. The microcontroller then generates a stream of 16 bit binary words, each word corresponding to the start of a pulse from the toothed wheel. Pulse period

is calculated on-the-fly by observing the difference between consecutive words. By inverting each pulse period, a new 16 bit word proportional to shaft angular is obtained.
The limitation of this method is that when shaft is derived from the inverse of the pulse period, there is an implicit minimum (but non zero) detectable velocity. Following this discussion, the minimum velocity specification is set to 20 rpm. Maximum velocity specification is equal or higher than 2000 rpm.
Design detail for speed shaft encoder can be found in [20] [37].

5-4, Power circuit.

Schematic for power inverter is shown in fig 5.24. It contains an uncontrolled diode rectifier, the filter capacitor and inductance on dc link and transistor inverter, including anti-diodes.

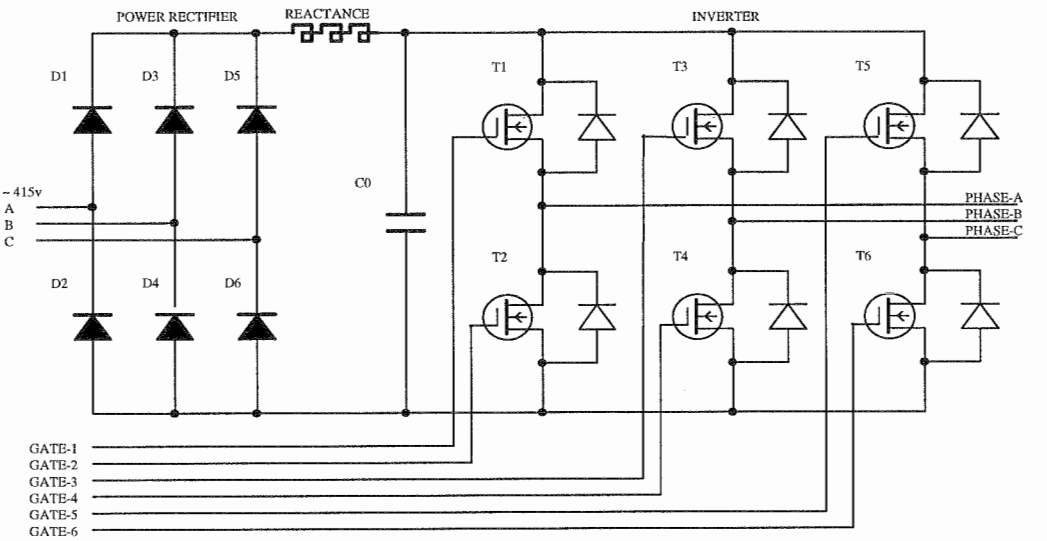


Fig 5.24, Power circuitry.

The inverter has the required capability of supplying a load with maximum current 10A. In addition, when transistor is turn off, the dc voltage Vd will applies on collector-emitter gate of transistor. Hence, the collector-emitter voltage gate of each transistor, when base-gate is opened, should be chosen two time bigger than the maximum dc voltage.
The operating frequency of transistor is chosen at least 2 kHz to ensure safety of transistor at switching time when inverter acts at low frequency.
Although BJT's can be utilised as the switching component for power inverter, the power MOSFET's are chosen to because these devices are used in modern drives.

Chapter 6 : System Software implementation.

6-1, General of the system software operation.

The flowchart of the system software is shown in fig 6.1. It includes six interrupt service routine in which the interrupt level 5 contains selected mode, speed and current control procedure and interrupt level 6 contains current control and PWM procedure.

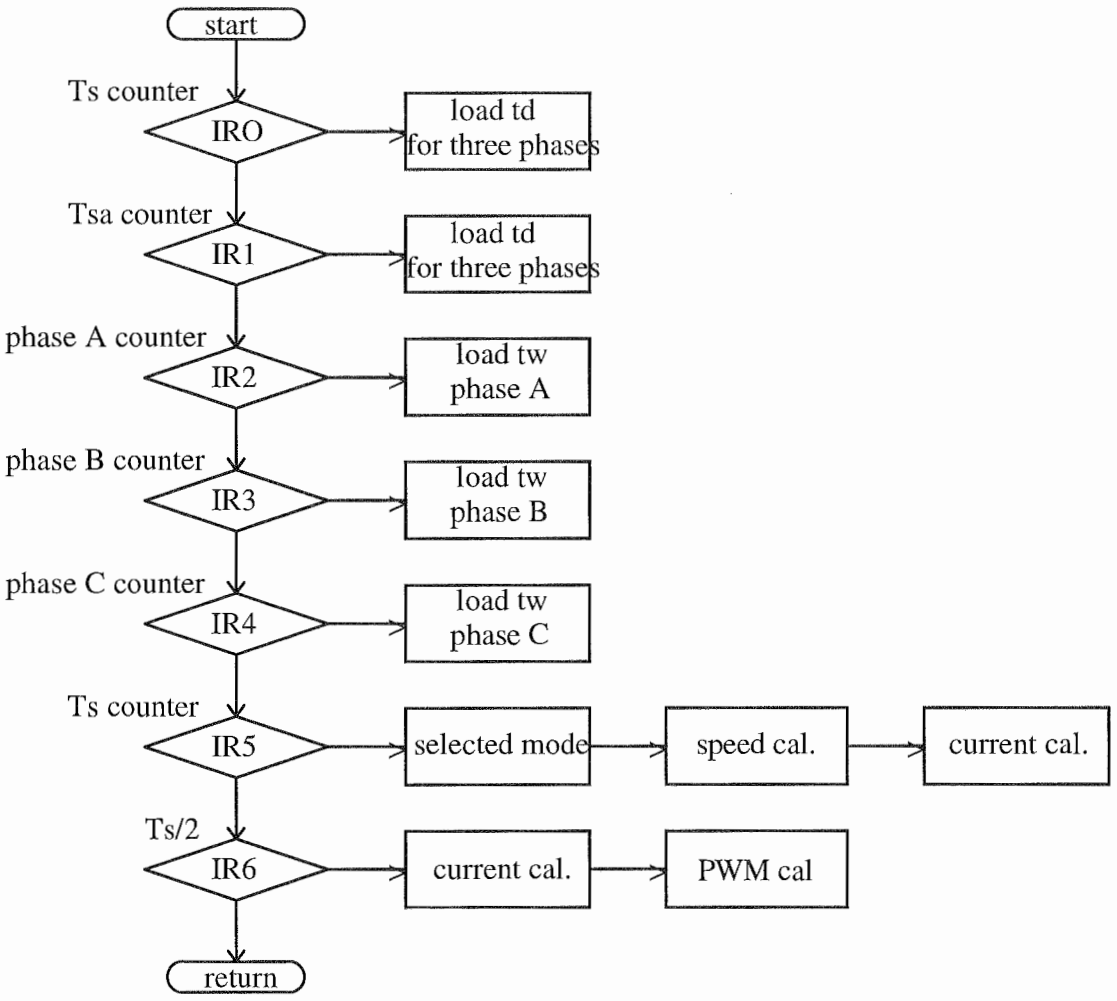


Fig 6.1, Flowchart of system software

The operation of the system software can be explained as follow : at the leading edge of the sampling interval Ts, an interrupt pulse active interrupt level 0. As a result, the ' load td ' interrupt service routine loads the time delay td to the respective phase counter simultaneously. Then, the interrupt level 5 is active. The selected mode , speed and current control procedures are executed consequently. At the same time, the CPU of microcontroller continuously checks if phase counter is clear. If phase counter is clear, the interrupt level 3 (or 4, 5) is active. This interrupt automatically loads the pulse width time tw into phase counter. At the half of the sampling period Ts/2, a pulse is issued to active interrupt level 6. The current control procedure is repeated

and then the PWM procedure is executed to calculate time delay td and pulse width time tw that are loaded into respective phase buffer to use in the next sampling period. At the end of the second time delay interval, the phase counter interrupt are supersede by the Ts interrupt to maintain synchronisation.

6-1-1, Selected mode procedure :

Fig 6.2 gives the mode transition diagram which shows the permissible transition between various modes and submodes at different condition of frequency. A hysteresis band of 1 Hz is provided between the adjacent states to ensure smooth transition.

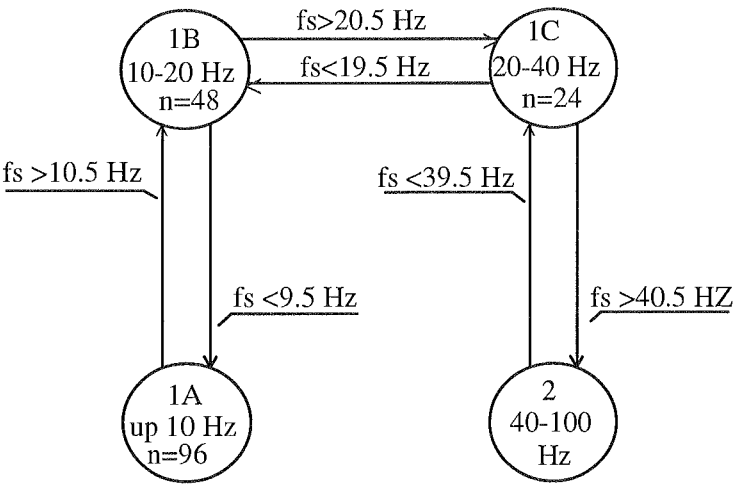


Fig 6-2, diagram of the selected mode procedure.

6-1-2, Speed procedure.

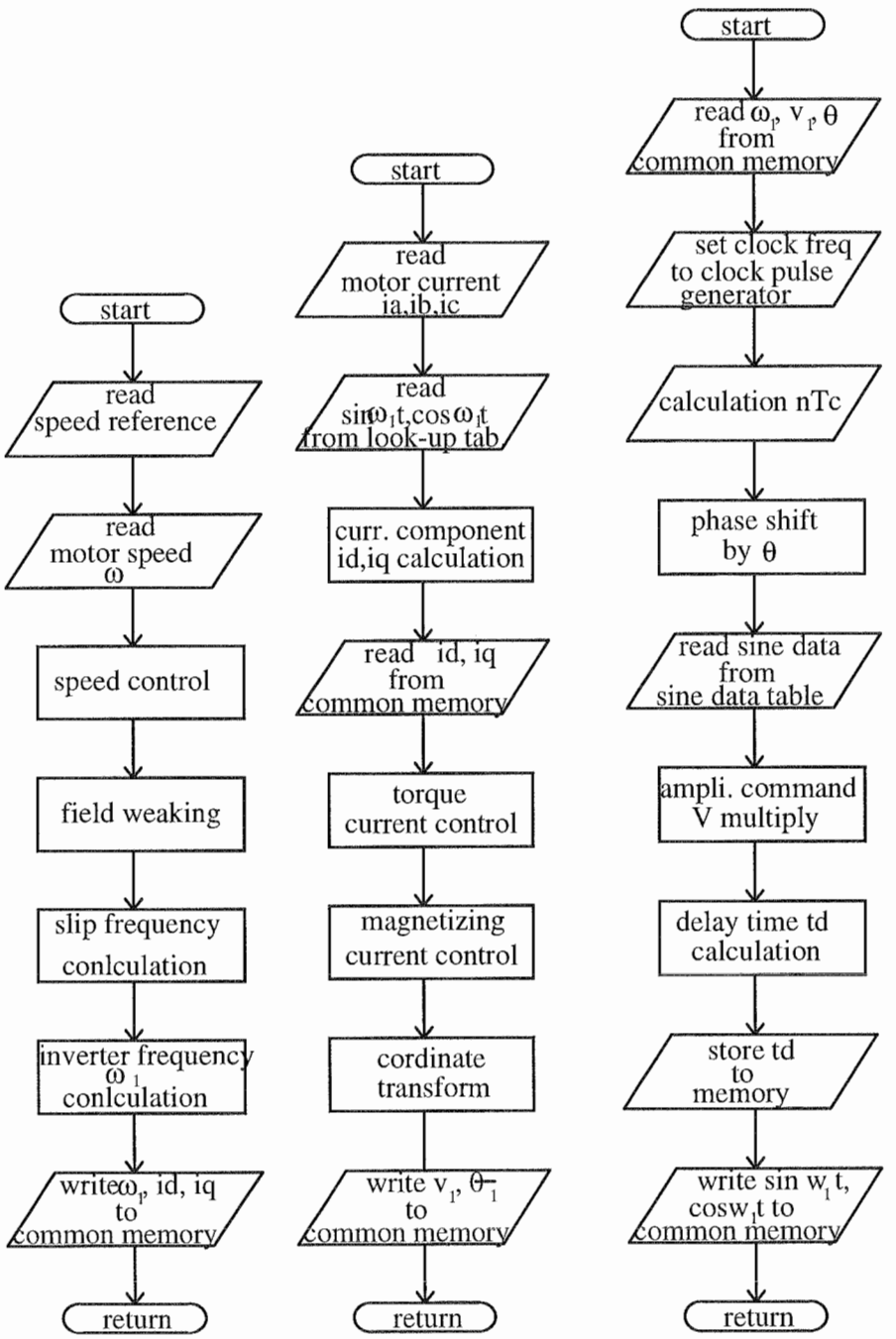
Flowchart of the speed procedure is shown in fig 6.3(a). This procedure is concerned mainly with speed control algorithm. It reads and processes the motor speed reference ω^r to produce the torque and magnitude current references. Then, the slip angular frequency reference ω^r_{sl} is calculated with eq (5.1) and added to motor speed to obtain the PWM inverter angular frequency reference ω^r_1 with eq (5.2). Finally, these processed result ω^r_1, i^r_{1d} and i^r_{1q} are written into RAM memory.

6-1-3, Current procedure.

Current procedure is executed twice in the sampling period Ts. First, it is executed soon after speed procedure is terminated. second, it is executed at the half of the sampling period. At the beginning of the current procedure, three phase motor currents are reads from A/D converter. These currents are processed to produce motor current components i_{1d} and i_{1q}. Then, the current references i^r_{1d} and i^r_{1q} are read from memory and compares with motor current reference to produce amplitudes of the voltage component references V^r_{1d} and V^r_{1q}. These voltage component are then converted to amplitude and phase of the real time voltage reference V^r_1 and θ^r_1 by using eq (5.3) and (5.4) and stored in RAM memory.

6-1-4, PWM procedure:

PWM procedure is used to calculate the time delay td and pulse width tw. The flowchart of the PWM procedure is shown in fig 6.3 (c). In executing, it reads reference values ω_1^r, V_1^r and θ_1^r from RAM memory and set clock pulse ts and Ts proportionally to values ω_1^r . Then, real time angular frequency values $\omega_1^r t$ is calculated by determining nTs.



(a) speed (b) current (c) PWM

Fig 6-3, Flowchart of the speed, current and PWM procedure.

The phase of the modulation signal is determined by adding values θ_1^r to values $\omega_1^r t$. The instantaneous amplitude of real time voltage reference v_1^r is than read out using

look-up sine data table stored in EPROM. From this value, the delay time td and pulse width time tw are calculated by eq (4.70) through (4.10) and stored in RAM memory. The instantaneous values of values $\sin\omega_1^r t$ and values $\cos\omega_1^r t$ are also read out from look-up table and stored for use for current detection in next sampling period.

6-1-5, Load td and tw interrupt service routine.

The flowchart for loading delay time td and pulse width tw is shown in g 6.4.

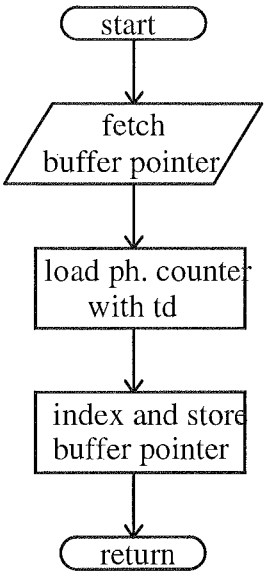


Fig 6.4, Flowchart of the load delay time routine.

6-1-6, Control algorithm :

In the speed and current procedure, some control algorithms must be specified for function of the PI speed and current controllers.

- The word for the delay and pulse time for three phase are computed and loaded into the respective phase buffer. These are then loaded into respective pulse width counter in correct instant of time.

Ref [13/p201] shows that an PI controller can be implemented in term of digital control. There are some algorithm to implement PI digital controller. This project employs the finite difference algorithm, in which the integration operator on the x variable is replaced by :

$$y_k = y_{k-1} + \frac{T}{2}(x_{k-1} + x_k) \qquad (6.1)$$

where T is sample interval.

From eq (6.1), The algorithms of speed and current controllers can be calculated and implemented by mean of software.

6-1-7, Estimated processing time.

The processing time for one sample interval is estimated for M68HC11 microcontroller as follows :

Procedure.	Processing time (μs)

Mode	50
Load time	50
Speed	150
current	250×2
PWM	200

It shows that total processing time is estimated 1000μs, or 1ms. Therefore, sample frequency, also carrier frequency, is limited below 1 kHz as mentioned in chapter 3.

6-2, Software implementation in C++

System software can be implemented in either assembly or high level languages such as C or pascal. However, high level language programs are much more convenience in comparing with assembly language :

* They are more likely to be self-documenting.
* The structure of the program can be made to reflect the structure of the original problem.
* Meaningful names can be chosen for variables and subprograms.
* The solution of the problem need not be obscured by the level of detail necessary in an assembler program.

From this point of view, high level languages are initial choice. Regarding that compiler for pascal is not available in lab, the C++ language is finally chosen to develop system software in this project.

All function of the PMW-IM drive system mentioned in previous chapters can be written in C++ language using Borland text editor. C++ program is then converted into an OBJ file by using HI-TECH compiler and subsequently, this file produces appropriate files contains binary code and the hexadecimal code. The hexadecimal code is required to ensure the conversion from mnemonics to machine code is correct.

6-2-1, Direct access of peripheral devices:

It is important to know the way a certain external device is accessed using C++ because each external device must be accessed, initialised and controlled when program is executed.

C++ provides two special functions, declared in header file <conio.h>, for accessing external devices [24]:

```
int   input (int  io_ port)        /* read a byte from io_ port */
int   output (int  io_ port)       /* write a byte to io_ port */
```

Here, ' io_ port' is defined as address of the external device including addresses of registers as a part of that external device. When called, *input* function return the byte read from the specified external device and *output* function write a byte to the device.

By using these function, data or status information of a certain device in IM control system, such as Ts and ts counter, parallel port, etc, can be passed between microcontroller and external devices via data bus. The addresses of each device can be found in the address mapping table 5.2, chapter 5.

6-2-2, Interrupt programming :

As shown in the fig 6.1, the system software contains 6 hardware interrupt. The service routines for each interrupt are explained in the previous section. From view

point of software implementation, these service routine must be first set up in the form of a interrupt procedure. This can be done in C++ by define [24]:

```
void  interrupt (far int_ procedure (void))
      {
            /* interrupt procedure body */
      }
```

The key word ' interrupt' tells the compiler that this is an interrupt service routine, The compiler will generate the appropriate entry and exit sequences including saving and restoring registers (in processor) and terminating the procedure with an IRET (interrupt return) instruction.
Next, the interrupt service routine is set to interrupt level of interrupt controller. C++ provides function *setvect* to do this job.

```
void  setvect (int  int_ number, void  interrupt ( * int_procedure)( ))
```

This function loads the interrupt level 'int-number, for the interrupt service routine *int_procedure* via its address.
All interrupt service routine of PWM-IM system software such as time delay calculation, speed and current procedure, etc, are written by using the functions explained above.

6-2-3, Initialisation for external devices.

As mentioned, all external devices must be initialised before main program is executed. Normally, each device interface contains a number of register which can pass data and status/control information between the program running in the processor and that device. Therefore, in order to initialise a device, its structure must be studied from data sheet. Then, mode word must be specified to each register of the device. finally, the concerning device can be initialise by transmitting a specified byte to its registers by mean of software.
In the software implementation of PWM-IM drive system, some care must be taken in initialisation for external devices :
+ All three port of the parallel interface are declared as output ports. Each output port must be kept low during the initialisation stage.
+ The phase counter is operated in MODE0 while Ts counter is operated in MODE3.
+ The interrupt controller is declared to be used in M6800 system. The interrupt input is unmasked. The interrupt vector table must be written in system RAM.
+ The communication interface must be reset.
Once initialisation is completed, the CPU will monitor the communication status register until the speed command is issued. On receiving data, the CPU loads the relevant counts to the system counter, sets the output logic ad the unmasks the interrupt enable flags to allow the CPU to accept interrupts. The CPU the simply service the interrupts of the system as they occur.

7-2-4, Communication programming.

The function of the communication programming is to send motor speed reference from host computer to the M68HC11 microcontroller and/or receives system status if drive is used in data acquisition system.

The communication subject is somewhat difficult to approach and beyond the scop of this project. This section only discussion general ideas of system communication, focus on communication programming in C++. However, detail studies can be found in ref [22], [23].

In order to transfer over long distance, data between host computer and microcontroller is transmitted in serial via RS-232 interface. Three terms often encountered on serial data communication are simplex, haft-duplex and full-duplex, that are the way data is transmitted. Some the other terms are related to structure of data to be sent : start and stop bit, parity bit and baud rate [22].

The project employs the simplex transmission in which data is transmitted only in one direction. However, half / full duplex transmission can be used if the drive is developed to be used in data acquisition system or CIM system.

To initialise the serial port (port D) of M68HC11 microcontroller, a mode word and then command word are sent to the addresses of status/control registers of port D. By such a way, number of start bit, stop bit , parity bit and baud rate are set to serial port of microcontroller. A procedure is then written for microcontroller to receive data from host computer, depending on status of the clear-to-send (CTS) pin.

The same way can be applied to host computer. However, the project employs an another method in which the serial port COM of computer is accessed, initialised and controlled via some special function of ROM BIOS. This method shows a simplification in programming and hence is discussed here.

The ROM BIOS provide four functions via interrupt type 14H for controlling serial ports (COM0: to COM3:). In all cases, register ah of CPU contains function numbers (0 to 3) and register dx contains the serial port numbers (0 to 3). A brief description of each function is presented as following :

Function 0 : is used to initialise serial port. The data word format is specify in register al of CPU.

bit 1,2 word length of processing data : 10 for 7 bits and 11 for 8 bits.
bit 2 number of stop bit : 0 for one stop bit and 1 for two stop bit.
bit 3,4 parity bit : 00 non, 01 odd, 10 non, 11 even.
bit 5,6,7 baud rate : from 000 for 110 baud to 111 for 9600 baud.

Function 1 : transmits data. Data to transmit is stored in al register. On returned, bit 7 of ah will be set if an error occurs and the remainder of ah contains line status.

Function 2 : receivers data. When called, this function waits for a character to be received. The character is then transmitted into al register. Bit 7 of ah indicates if any error occurs and bit 1,2,3,4 indicate the line status.

Function 3 : reads serial port status. It returns the values of the line status in ah register and modem status in al register.

In order to access ROM BIOS function for serial communication, C++ provide function *int86*. When *int86* function is called, information is passed to 16 bit processor register ax,bx,cx,dx,si and di or their byte equivalent. In Turbo C++, the function prototype of *int86* is declared in header file < dos.h > thus :

```
int int86 ( int int_number, Union REGS * in_register,
                            Union REGS *out_register );
```

Where :

int_number is the interrupt type to invoke the required MS-DOS functions.
int_register is the value of the CPU register to be passed to MS-DOS.
out_register is the value of the CPU registers as returned by MS-DOS.

The declaration of Union REGS is of the form:

```
/* Intel 8086 family word register ( 16 bit ), cflag is the carry flag */
  Struct  WORD_REGS { Unsigned int ax,bx,cx,dx,si,di,cflag };
/* Intel 8086 family byte registers (8 bit ) */
  Struct  BYTE_REGS  {  Unsigned char al,ah,bl,bh,cl,ch.dl,dh};
/* Intel 8086 general purpose registers : overlap word and byte registers */
  Union  REGS  {
                    Struct  WORD_REGS       /* Word registers */
                    Struct  BYTE_REGS       /* Byte register */
```

Using variables of type Union REGS, a CPU register may be accessed as a 16 bit word or a pair of 8 bit byte.

By accessing serial port via BIOS functions shown above, one can write program to transmit and receive data from host computer. An example to initialise serial port COM: of the host computer is given in fig 6-6.

```
/* Procedure to initialise 8250 port number " io_port " with 8 data bit, no parity,
one stop bit and 9600 baud. */
 void rs_initialise ( const int io_port )
 {
   Union  REGS  register ;                  /* variable to hold 8086 register */

   register.h.ah = 0 ;                      /* initialize function 0  */
   register.h.al = 0xe3 ;                   /* set data bit, parity bit, stop bit, baud */
   register.x.dx =io_port ;                 /* specify port number */

   int86 ( 0x14, & register, & register ); /* call interrupt type 14H */
  }
```

Fig 6.6, Procedure to initialise io_port

There are some advantages of using ROM BIOS functions. First, they may save programming efforts and space in the program file. Second, they make program more compatible with other DOS machine. Finally, programs using DOS and BIOS functions exclusively could be compatible with future versions of the PC.

Chapter 7 : Experimental Result and Evolution

7-1, Experimental results.

Three breadboards are built in the laboratory for the system operation in the frequency range 5 to 100 Hz. The printed circuit boards are designed by using the Protel Schematic and Autotrax editors with the help of the technician staff of the Department of the Electrical and Electronic Engineering. Schematic drawings of the system hardware are shown in appendix C. The inverter circuit and main part of the modulator are built and tested by using an IBM-PC insteads of M68HC11 microcontroller. The system under test is shown in fig 7.1. It can be seen that an another computer is included for measuring motor parameters using Boston Technology PC30 Card and STATUS-30 Software. In addition, a three phase generator is used as motor load. The system under test is shown in fig 7.1.

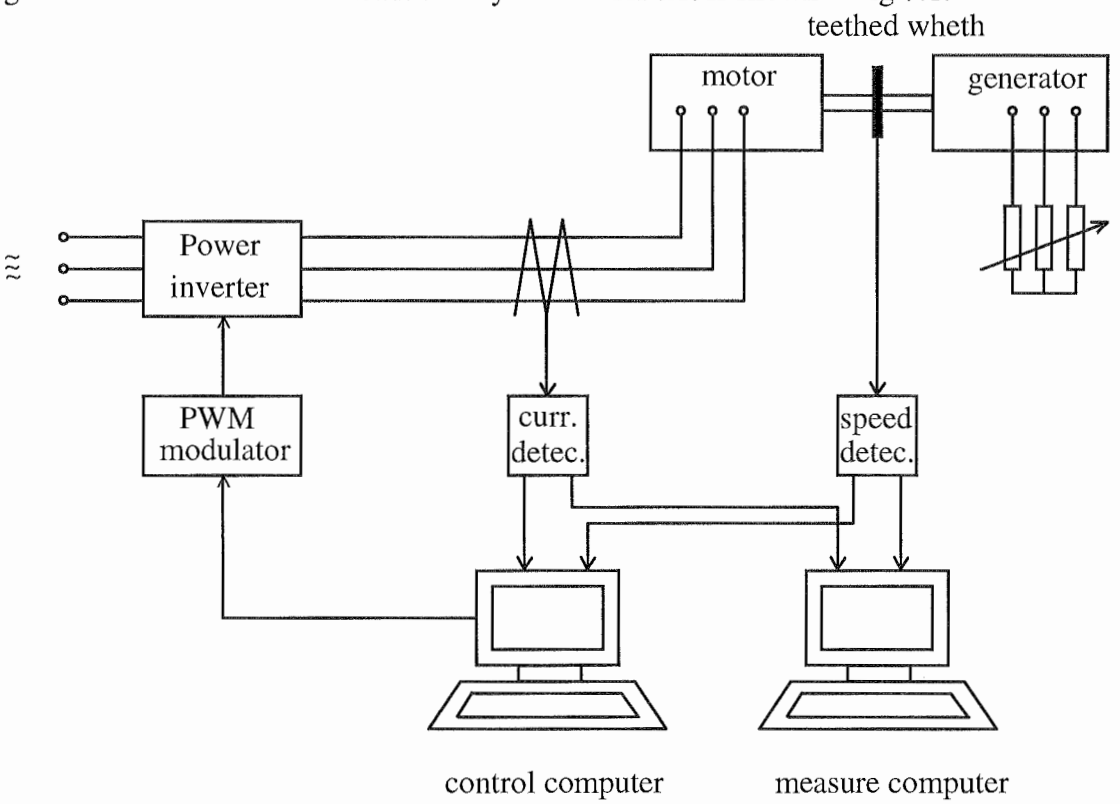


Fig 7.1, Configuration of system under test.

The motor line voltage and currents are measured at 40, 20 and 5 Hz. Because the speed of the IBM-PC is much faster than M68HC11 microcontroller, the maximum carrier frequency fc can be increased up to 2 KHz, ie the number of sample n in each period of the modulating waveform can be increased twice (n=48, 96 and 192).

The results for open loop are shown in 7.2, 7-3, and 7.4. It can be seen from voltage frequency spectrum that the harmonics perform several bands centred around nth harmonic and its integer multiplied harmonics (2nth, 3nth ...). However, the amplitudes of the nth harmonic and its integer multiplied harmonics are zero. This is explained that in the synchronous mode, the carrier frequency is multiple of 6 of the fundamental frequency in the modulating wave (eq (4.5)). As a result, nth harmonic and its integer multiplied harmonics must be eliminated.

From this point of view, the harmonic with highest amplitude must occur around nth, 2nth, 3nth and so on. That are 48th, 96th, ... harmonics when system operates in the synchronous mode.
The current harmonics are much smaller than that of the voltage harmonics because of the act as low-pass filter of the motor magnetising reactance
The closed loop has not been tested. However, a problem could be arisen. That is the closed loop processing time seems to be longer than estimated. In such a case, the maximum carrier frequency must be reduced, or some control procedure must be written in assembly language to reduce processing time, or M68HC11 must be replaced by another microcontroller with faster speed.

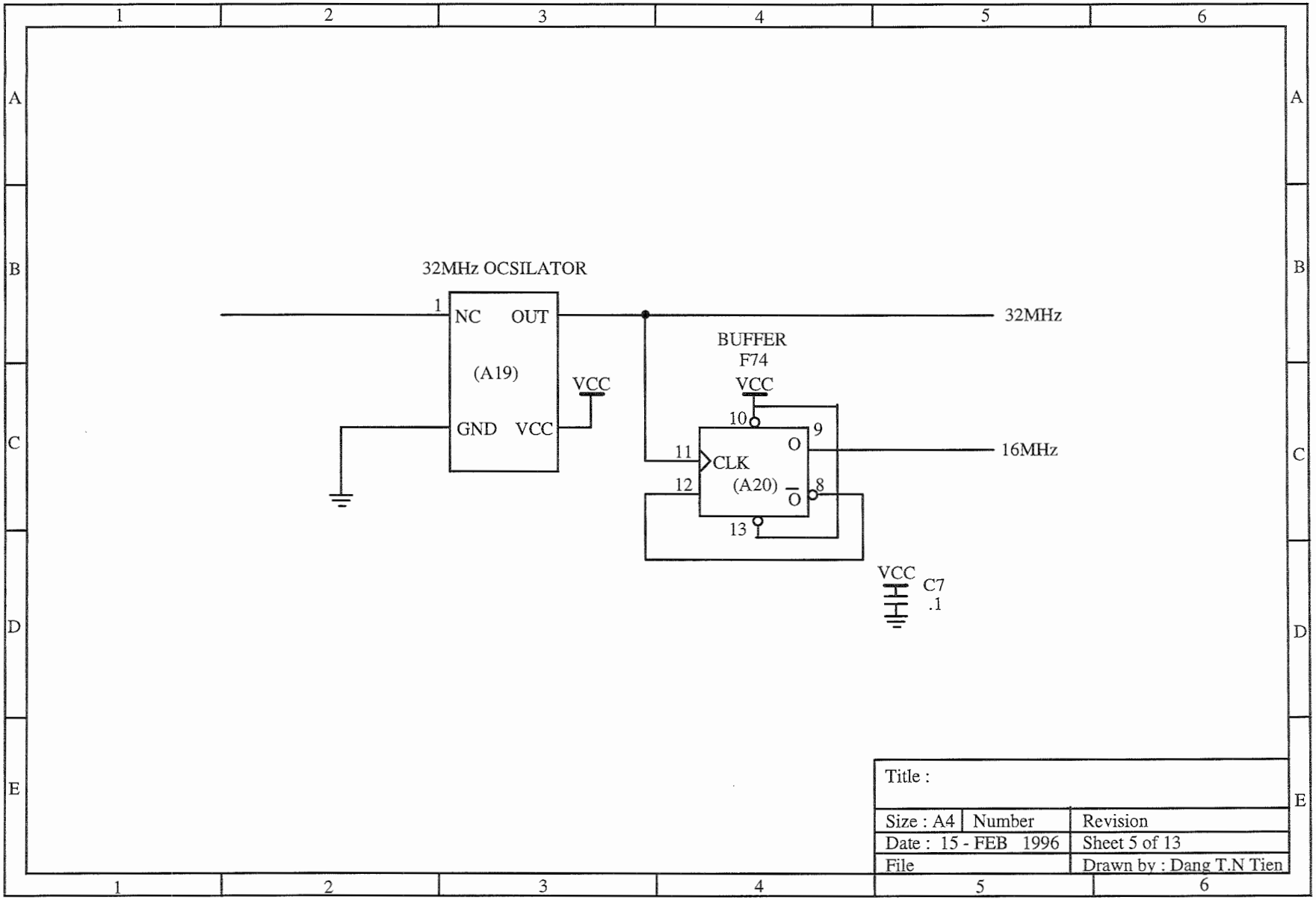


Fig C.5. Ocsilator

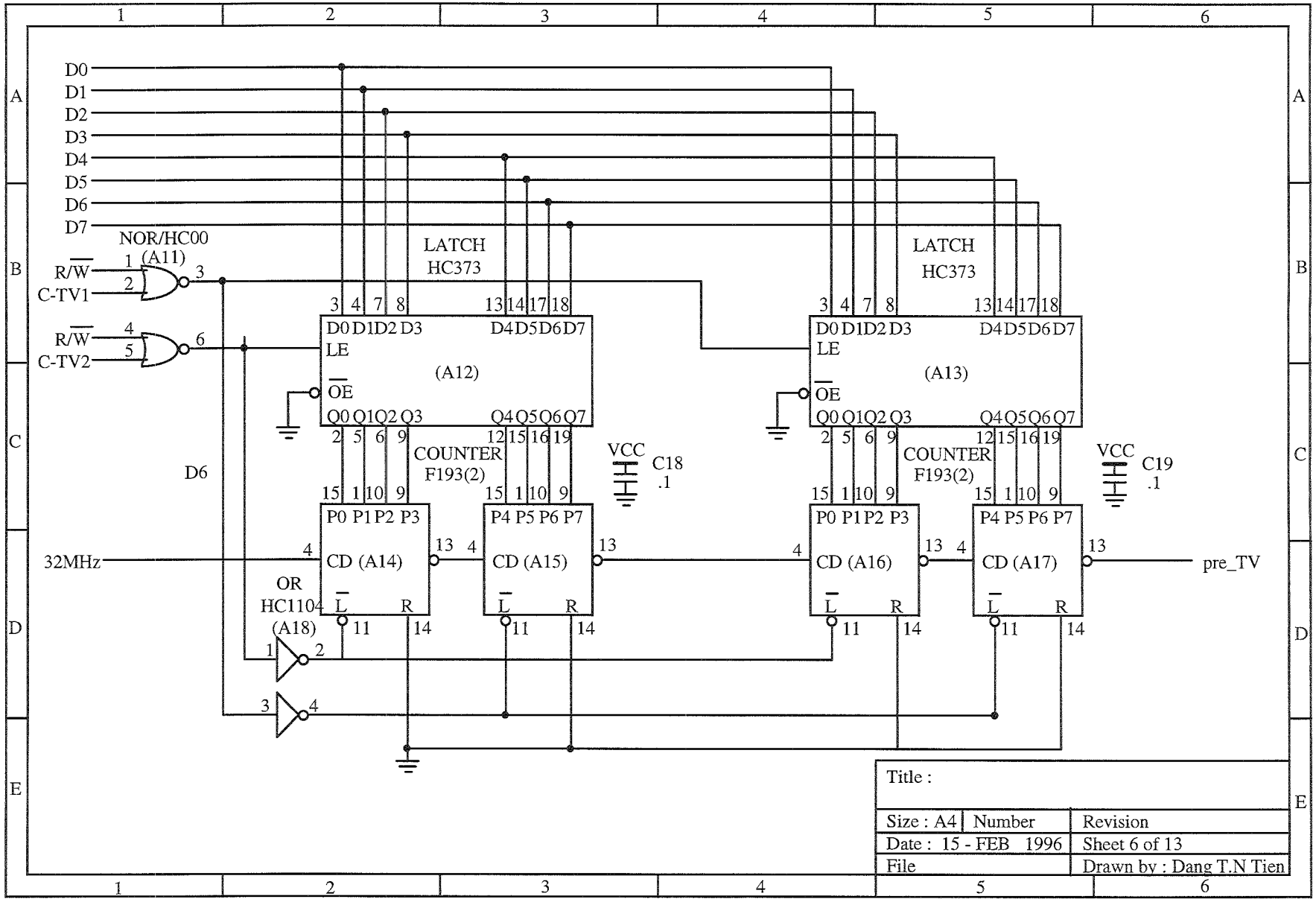


Fig C.6, 16 bit Tv counter circuitry

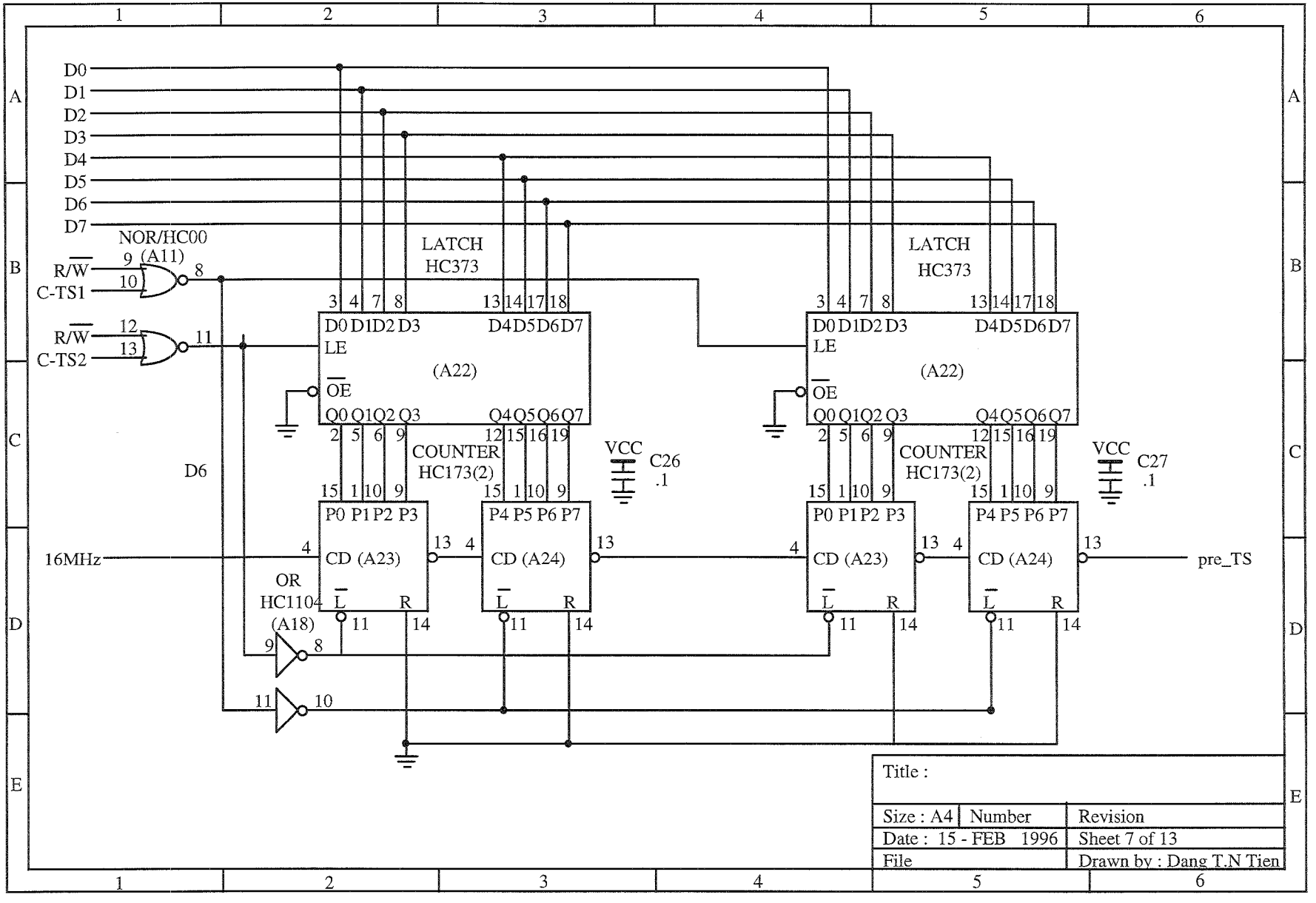


Fig C.7,16 bit Tc down counter circuitry

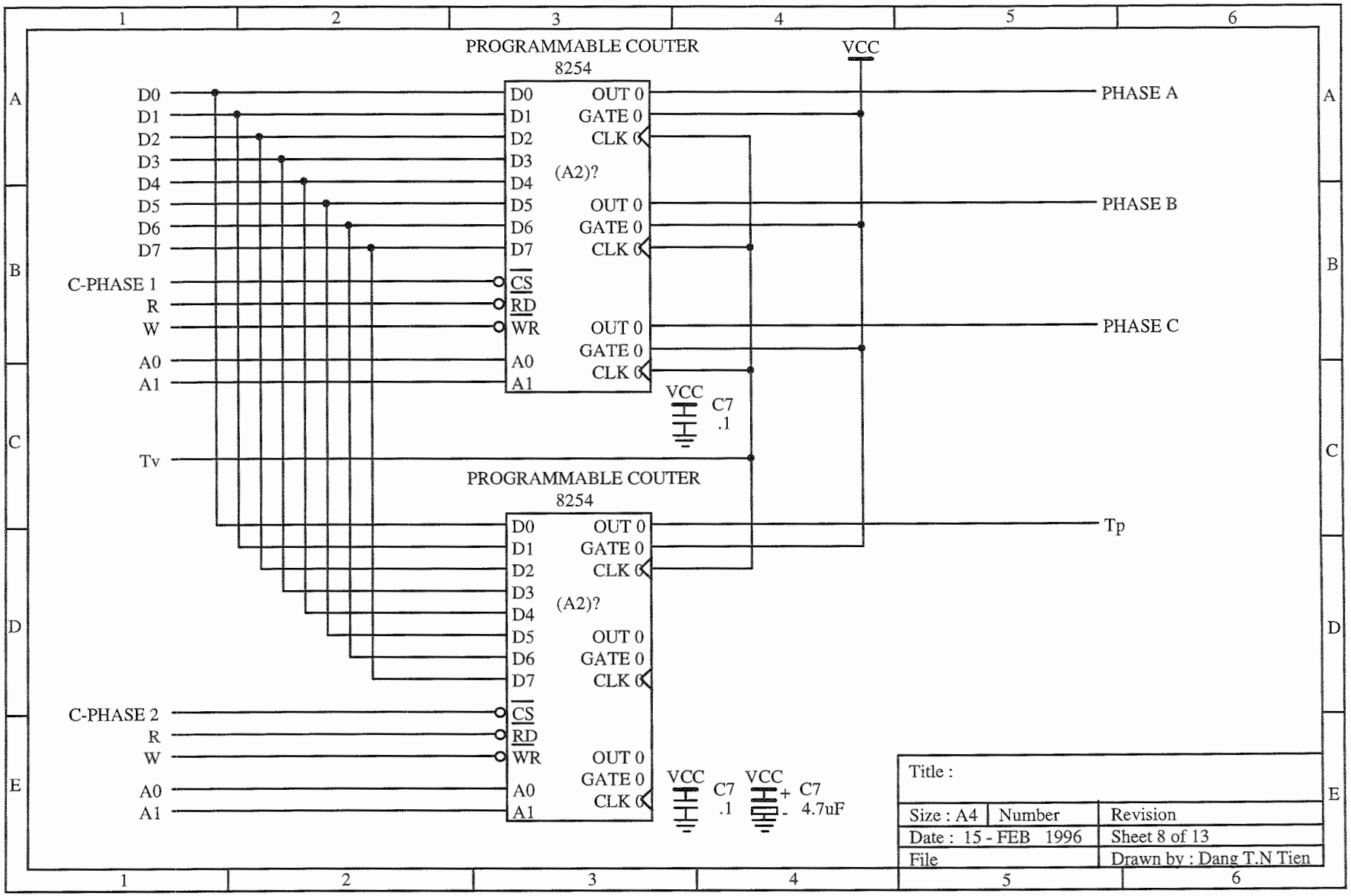


Fig C8, Programmable counter

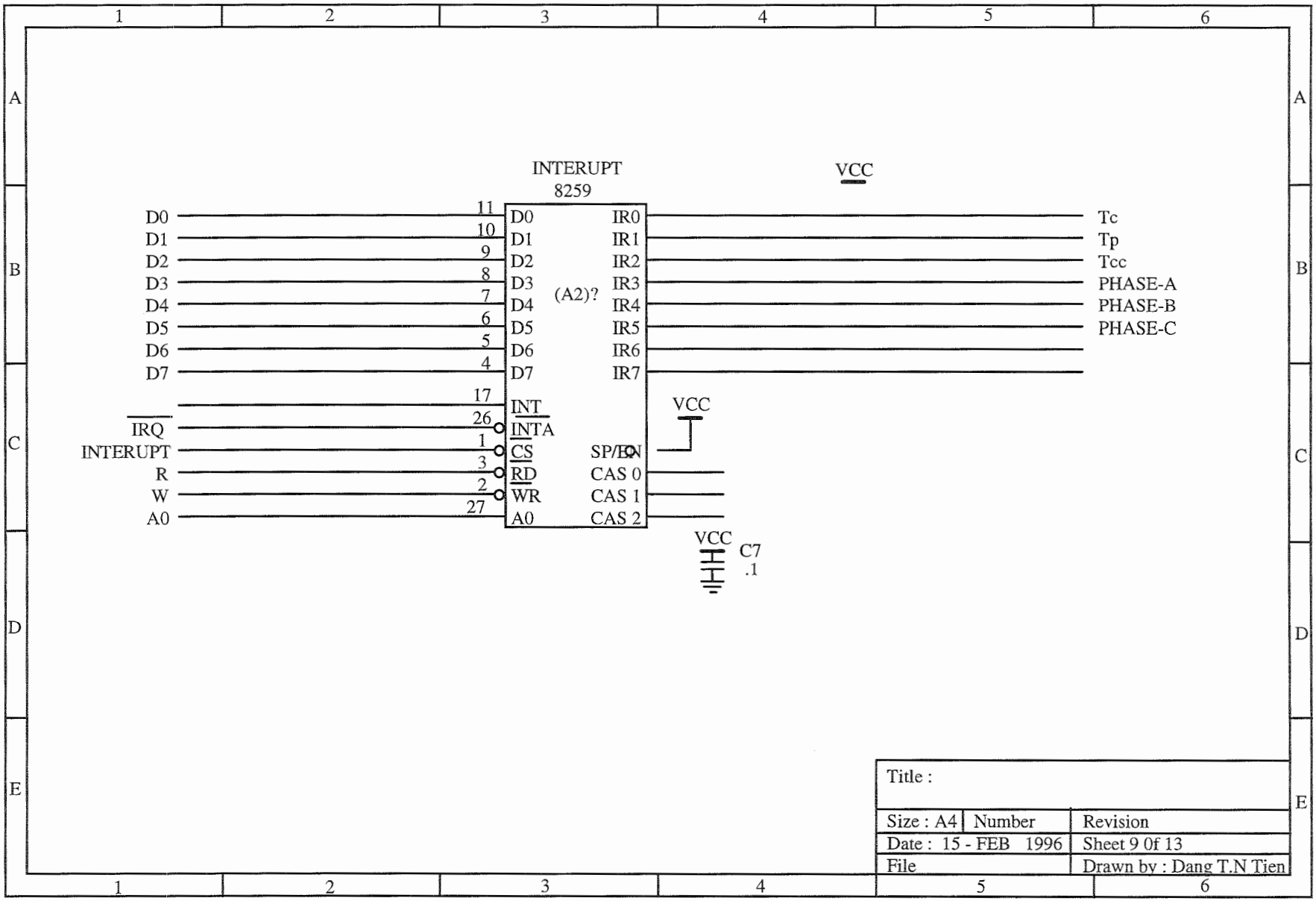


Fig C.9, Interrupt circuitry

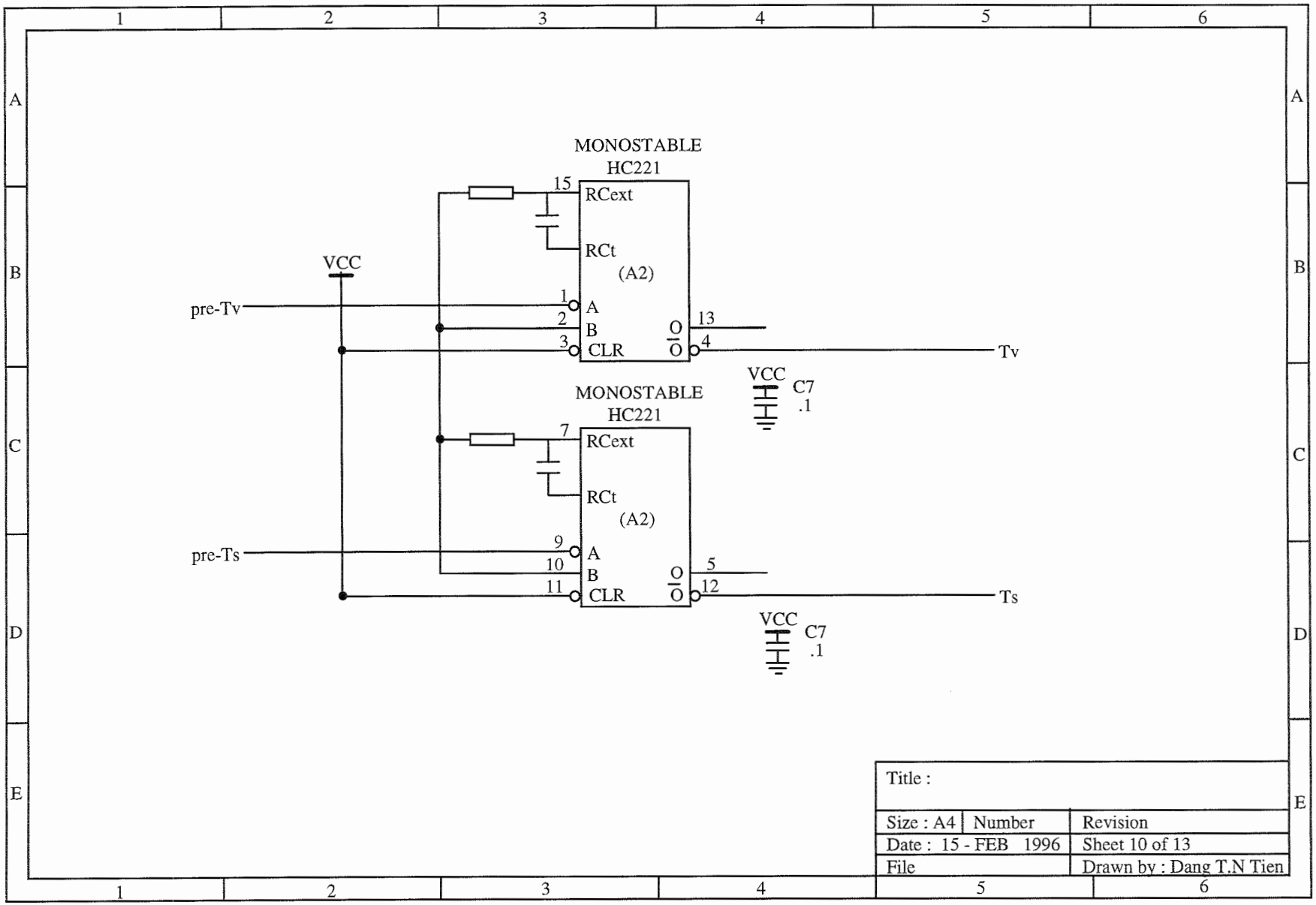


Fig C.10, Monostable circuitry and ocsilator

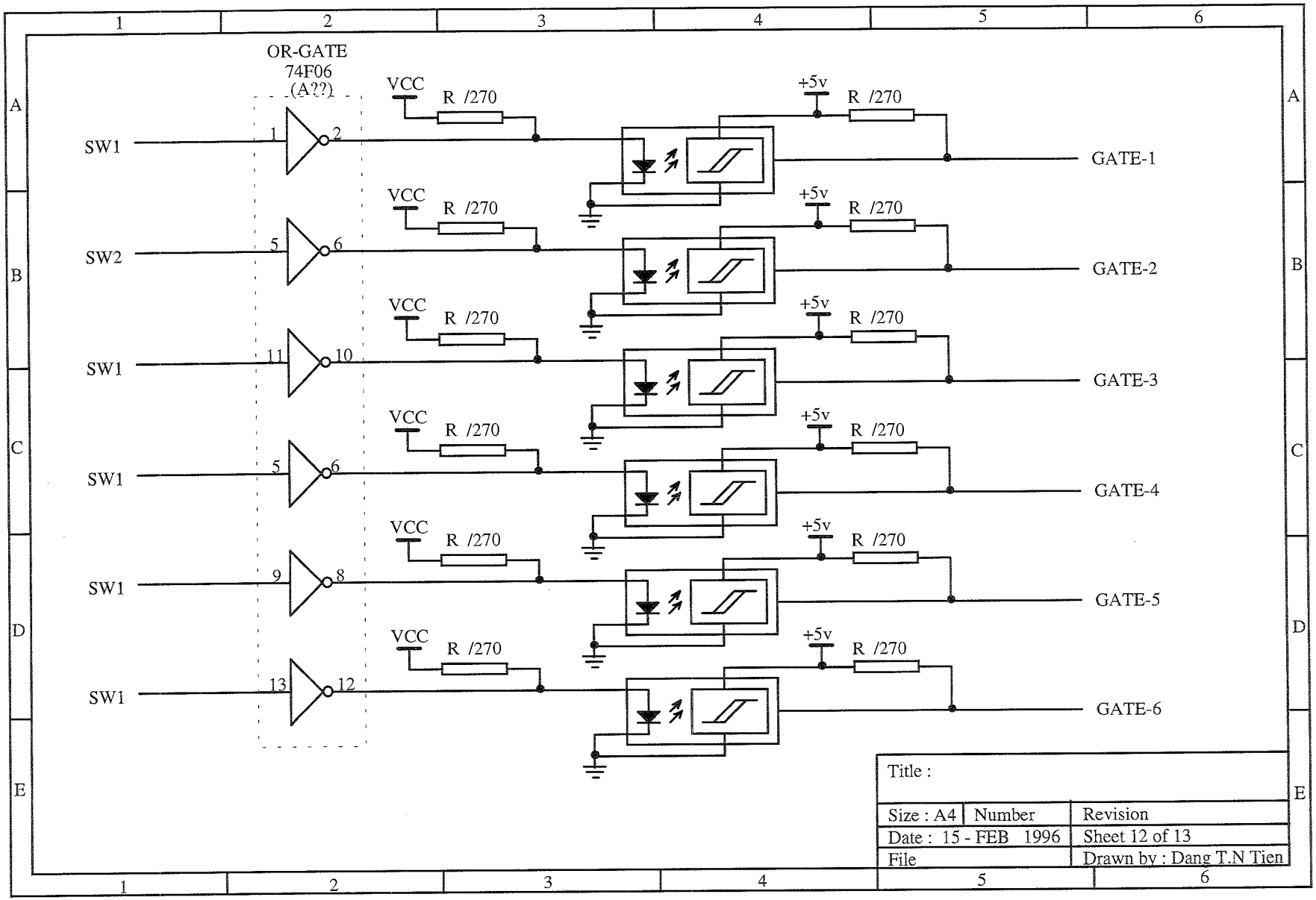


Fig C.12, Isolation circitry

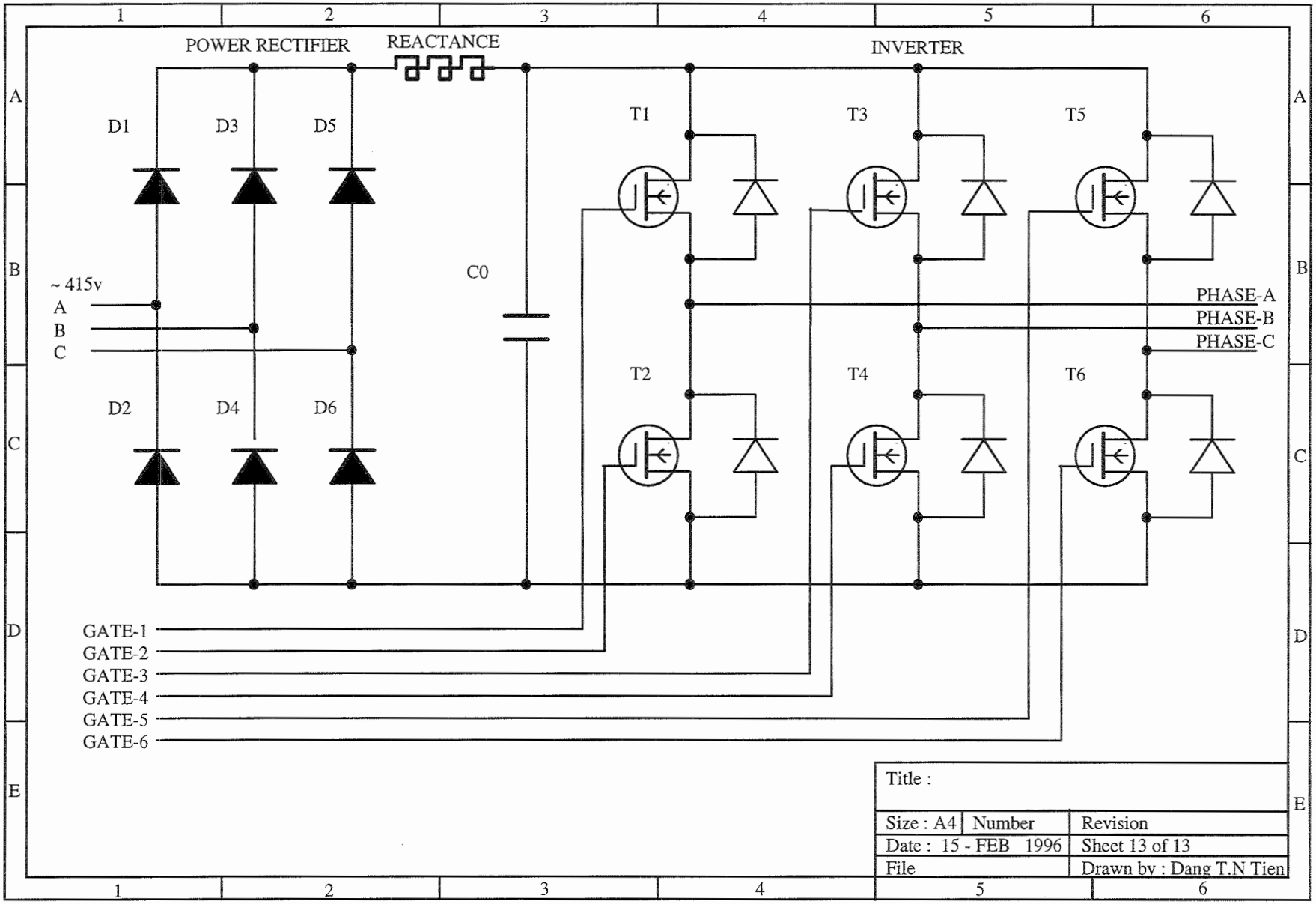


Fig C.13, Power circuit